Design of an Adaptive Biasing Circuit to Improve the Dynamic Performance of CMOS Op-Amps Operating in Subthreshold Region

A Thesis Submitted

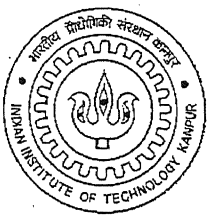
in partial fulfillment of the requirements

for the Degree of

Master of Technology

by

GIRISH KURKURE



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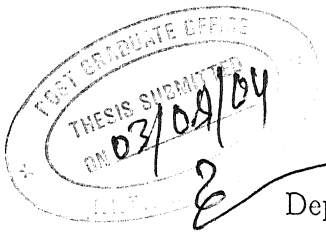
CERTIFICATE

It is to certify that the work contained in this thesis entitled **"Design of an Adaptive Biasing Circuit to Improve the Dynamic Performance of CMOS Op-Amps Operating in Subthreshold Region"**, by Girish Kurkure, has been carried out under my supervision and guidance. This work has not been submitted elsewhere for the award of any degree.



(Dr. Aloke Dutta)
Professor
Department of Electrical Engineering
Indian Institute of Technology
Kanpur, India

IIT Kanpur
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Abstract

For low power applications, it is required that the stand-by power consumption of the circuits should be very low. In order to achieve this, circuits can be operated at very low current levels by operating the MOSFETs contained therein their subthreshold mode of operation. However, this severely affects the dynamic performance of the circuits, in particular, the transient response and the slew rate. In this work, a new adaptive biasing scheme for differential amplifiers (DAs), operating in the subthreshold region and thus suitable for low-voltage and low-power applications, has been proposed. This circuit provides an additional bias current, over and above the normal bias current for the DA, which is proportional to the differential signal between the two inputs of the DA, thus having the prospect of improving the dynamic response. The designed circuit has been used in an Operational Transconductance Amplifier (OTA) with ± 1 V power supply, and it has been shown that the positive slew rate has improved from 2.92 V/μs to 1242 V/μs, and the negative slew rate from 1.5625 V/μs to 133 V/μs. At the same time, the small-signal performance parameters (i.e., gain margin and phase margin) remained almost the same as that without adaptive biasing (as expected), and there was a small decrease of the dynamic range [(+913 mV to −915 mV) from (+907 mV to -902 mV)]. The most useful feature of the proposed biasing circuit is that it requires negligible amount of stand-by power as compared to the previously developed circuits reported in the literature. This reduction in the stand-by power is due to the fact that no additional quiescent current source is required in the proposed circuit, unlike those reported earlier.

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Chapter 1

Introduction

The need for high speed CMOS integrated circuits led us towards continuously reducing minimum feature size of MOS devices. The capacitances associated with the MOS devices are proportional to the device dimensions, and if the current drive capability of the devices is kept constant, then the circuit with reduced capacitances is faster in response, and, hence, will have larger bandwidth. However, very large bandwidth may not be needed for every application, e.g., there are situations where one can be satisfied with smaller bandwidth but can not afford large power dissipation, because larger the power dissipation more frequent will be the need for replacement of the batteries. Pacemaker is a good example which illustrates this trade-off.

With both Full Voltage Scaling and Constant Voltage Scaling of MOS devices, the power dissipation per unit area either remains constant or increases by the scaling factor respectively [1], making power dissipation in these circuits a prime concern. Hence, in recent years, many efforts have been made for reduction of both the supply voltage as well as the power consumed by the MOS circuits. The correct operation of analog circuits at low voltages demands exploration of new blocks, new circuit topologies, and new techniques which can reduce overall power dissipation per unit

area without sacrificing other parameters too much. The two most common techniques to reduce the overall power dissipation are described below.

➢ **Low-voltage techniques** are basically related to the operation of devices with the minimum possible supply voltage, while keeping them in the strong inversion region of operation. This minimum required voltage is given by $|V_{DD} - V_{SS}| \geq V_{TN} + |V_{TP}|$, where V_{TN} and V_{TP} are the threshold voltages of the NMOS and PMOS devices respectively, and V_{DD} and V_{SS} are the positive and negative power supply voltages respectively [2]. However, in these techniques, the reduction in power is not significant since the order of current remains almost the same as before.

In order to meet the low power requirements, several approaches have been proposed in the literature which use low power supply voltages. Two typical examples of these approaches are the floating-gate transistors [3,4], and the bulk-driven transistors [5]. Both techniques have individual drawbacks. Floating-gate transistors have a smaller transconductance g_m and a larger output conductance g_{ds}, as compared to those of conventional transistors. Bulk-driven transistors were first proposed by Guzinski [6]. It is possible to overcome the threshold voltage limitation (given by $|V_{DD} - VSS| \geq V_{TN} + |V_{TP}|$) by using bulk-driven techniques, since in these techniques, the gate-to-source voltage only sufficient to form the inversion layer is required, and the drain-to-source saturation voltage is less than that under gate-driven case [6]. Bulk-driven transistors experience a reduction in the gain-bandwidth product and a worse frequency response because of substantially smaller transconductance, which in effect is the body transconductance g_{mb} instead of g_m for the gate-driven case. Moreover, bulk-driven techniques can only be applied to devices that can be fabricated in their own wells [7].

➢ **Low-voltage low-power techniques** are used to operate the devices

well below the $V_{TN} + |V_{TP}|$ limit. Thus, in these techniques, the MOS devices are operated in their subthreshold region of operation, where the order of current is significantly lower than that under strong inversion region of operation. Thus, the power dissipation is also considerably less than that under low voltage operation.

The use of the low biasing current, which ensures reduced power consumption, severely limits the transient characteristics of op-amps, in particular, the slew rate (for large signal) and the gain-bandwidth product (related to small signal). For this reason, it is necessary to have a trade-off between speed and power dissipation. Speed is one of the most important properties of analog circuits. The speed of high performance mixed signal systems are mainly determined by the settling time of the op-amp [8], which is defined as the time required for the outout of the op-amp to reach within 2% of its final value.

The settling response of op-amps consists of two distinct parts: (1) the slew rate limited period, and (2) the small-signal settling period [9]. The first part of the step response behavior (i.e., the slew rate limited period) is obviously governed by the slew rate, which is a first order parameter affecting the speed, and the second part (i.e., the small-signal settling period) is determined by the location of the poles and the zeros. In order to enhance speed, the slew rate of the op-amp should be increased. In order to achieve high slew rate, it is required that the amount of current available to the biasing current source of the differential input stage of the op-amp should be able to charge and discharge the load capacitor within the shortest time. Simple techniques of increasing the magnitude of this biasing current are detrimental due to large consequent power dissipation problem. Reduction of this biasing current, on the other hand, worsens the dynamic characteristics, however, there are many applications where the input variations are present only during very short time intervals (for example, in the case of sample and hold circuits), and, consequently, a high driving capability is required only

for a very short time.

A possible solution to optimize these two circuit performance constraints, i.e., speed as well as power dissipation, is to utilize adaptive biasing [10]. In this technique, the concept of an input dependent bias current source is introduced, which results in a very low stand-by power dissipation with good dynamic characteristics. In the literature, several designs of adaptive biasing circuits have been reported [7-12], however, almost all of these require additional quiescent current sources, and, thus, stand-by power consumption becomes considerable. At the same time, these adaptive biasing circuits provide large dynamic power to the op-amps only on the application of the input signals, thus improving their dynamic performance. Only the novel adaptive biasing circuits presented in [13] and [14] do not require any additional quiescent current sources, except for situtations where the sensitivity of the circuit needs to be improved.

In order to meet low voltage and low power requirements simultaneously, we have chosen to operate the devices in the subthreshold region of operation, and, thus, succeeded in getting lower power consumption with lower supply voltages. Operating the devices in the subthreshold region of operation has resulted in larger low frequency gain, while on the other hand, the bandwidth and the slew rate have suffered a loss, for obvious reasons. In order to eliminate this problem, this work has concentrated on the design of a CMOS biasing circuit that operates in the subthreshold region of operation, is able to bias the op-amp and the operational transconductance amplifier (OTA) adaptively, and, thus, improves the slew rate and lowers the power consumption as compared to the already existing topologies [9,10]. In order to ensure low stand-by power dissipation, another aim of our design process was to design the adaptive biasing circuit without additional quiescent current source requirement.

The organization of the thesis is as follows. The derivation of the subthreshold current equation [15] and the current-voltage characteristics of an NMOS device in the subthreshold region of operation are presented in Chapter 2. The small-signal model valid in this region of operation is also discussed in this chapter with a description of the model parameters. Chapter 3 discusses the operation of the differential amplifier (DA) in the subthreshold region of operation. The reason for the slew rate limitation [16] is also given here. Already existing techniques in the literature [10,11] for slew rate improvement are explained. Chapter 4 deals with the adaptive biasing circuit proposed in this work here in order to improve the slew rate of the DA, and the simulation results of an OTA using this proposed circuit are compared with the results obtained for the same OTA biased with a constant current source. The TANNER EDA tool [20] has been used for all the simulations with 0.5 μm technology file, supported by the BSIM 3v3 model [21]. Chapter 5 includes the summary of this work along with a discussion about the scope for future work. The MOS device data and the technology file are given in APPENDIX.

Chapter 2

Subthreshold Region of Operation of MOS Devices

2.1 Introduction

Op-amps operating in the subthreshold region of operation have become very popular lately, because they operate both at lower power supply currents as well as at lower power supply voltages. Hence, subthreshold region of operation is extremely productive for low power applications. This chapter revisits the derivation of the subthreshold current equation, as well as presents the simulation results for the current-voltage characteristics of an NMOS device. The small-signal model valid in this region of operation is also discussed along with an explanation of the various model parameters.

2.2 Development of the Subthreshold Current Equation

In semiconductor devices, the total current can be considered to be composed of two components, namely the drift component and the diffusion component. Same is the case with the drain to source current in MOS devices. The regions of operation of MOSFETs can be classified according to the dominance of

one of these components over the other. In the strong inversion region, the drift component dominates over the diffusion component, while in the weak inversion region, the reverse is true. The moderate inversion region is defined by the region where both these components are comparable to each other. In this section, we will rederive a generalized drain-to-source current equation, which is valid in all the three regions of operation, and later we will emphasize on the subthreshold region, the region of interest from low power point of view. This is done in order to get a better understanding of the subthreshold operation, and also to have a feel of the applicability of this region of operation in circuit designs.

Figure 2.1 shows the cross-sectional view of an n-channel MOSFET. Application of V_{GB}, the gate-to-body voltage, will cause opposite mirror charges to appear in the semiconductor. Practically all of these charges will be contained within a thin region adjacent to the top surface of the semiconductor. The development of the current equation is based on the charge sheet model [15], where the term charge sheet refers to the basic assumption that the inversion layer is of infinitesimal thickness. The current in the channel can be caused by both of the mechanisms, i.e., drift (I_{drift}) and diffusion (I_{diff}). Let x be the horizontal position in the channel measured from the source end. If the inversion layer current at x is denoted by $I(x)$, we will have

$$I(x) = I_{drift}(x) + I_{diff}(x) \tag{2.1}$$

The surface potential ψ_s at any position x is defined as the total potential drop across the region, from the surface to a point in the bulk. Application of a drain-to-source voltage causes ψ_s to become a function of x [15]. Now, consider a small element in the inversion layer between x and $x + \Delta x$, as shown in Fig.2.1. The potential difference across this element can be given by $\Delta\psi_s(x) = \psi_s(x + \Delta x) - \psi_s(x)$. Thus, the expression for the drift current

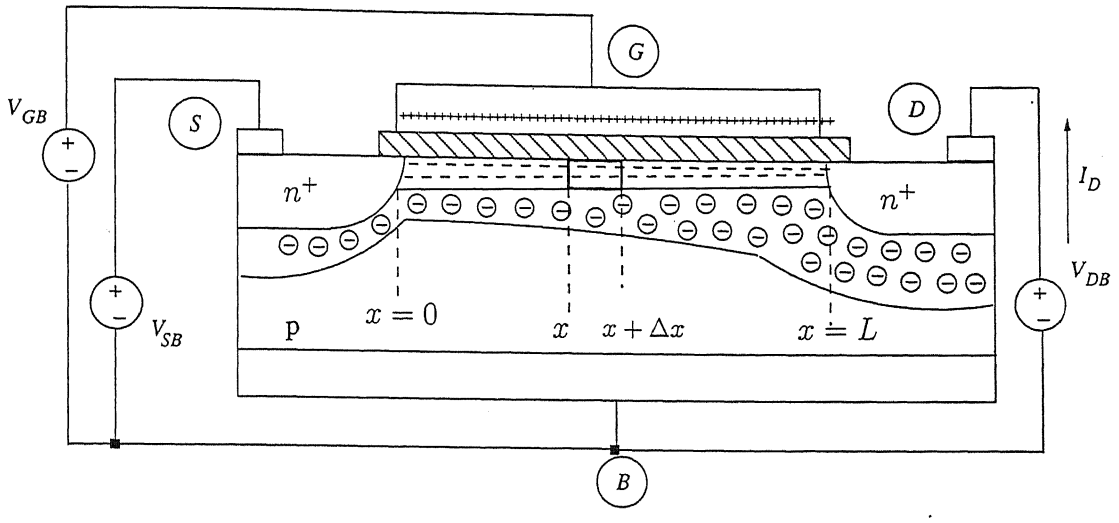

Figure 2.1. The cross-sectional view of an n-channel MOSFET.

component can be written as [15]

$$I_{drift}(x) = \mu W[-Q'_I(x)]\frac{1}{\Delta x}\Delta\psi_s(x) \tag{2.2}$$

where W is the width of the channel and μ is the surface mobility of electrons in this case. The term $Q'_I(x)$ is the (negative) inversion layer charge per unit area at x. Allowing Δx to approach zero, Eq.(2.2) becomes

$$I_{drift}(x) = \mu W[-Q'_I(x)]\frac{d\psi_s(x)}{dx} \tag{2.3}$$

The diffusion current component can be given as [15]

$$I_{diff}(x) = \mu W \phi_t \frac{dQ'_I(x)}{dx} \tag{2.4}$$

where ϕ_t is the thermal voltage, given by $\phi_t = kT/q$, with k being the Boltzman constant, q is the Coulomb charge, and T is the absolute temperature in Kelvin. In dc steady state, the total current I_D in the channel

must be the same for all x and equal to the drain current. Using this fact, we obtain

$$I_D = \mu W[-Q'_I(x)]\frac{d\psi_s(x)}{dx} + \mu W \phi_t \frac{dQ'_I(x)}{dx} \tag{2.5}$$

Let the surface potential at the source end of the channel (i.e., at $x = 0$) be denoted by ψ_{s0} and the inversion charge there by $Q'_{I,source}$. Let the corresponding quantities at the drain end of the channel (i.e., at $x = L$, where L is the channel length) be denoted by ψ_{sL} and $Q'_{I,drain}$ respectively. Now, integrating both sides of Eq.(2.5) from $x = 0$ to $x = L$, we obtain

$$\int_0^L I_D dx = W \int_{\psi_{s0}}^{\psi_{sL}} \mu[-Q'_I(x)]d\psi_s + W\phi_t \int_{Q'_{I,source}}^{Q'_{I,drain}} \mu dQ'_I(x) \tag{2.6}$$

Since I_D is independent of x, hence, it can be moved out of the integral. Thus, the left hand side of Eq.(2.6) becomes equal to $I_D L$, and after rearrangement, we get

$$I_D = \frac{W}{L}\Big[\int_{\psi_{s0}}^{\psi_{sL}} \mu[-Q'_I(x)]d\psi_s + \phi_t \int_{Q'_{I,source}}^{Q'_{I,drain}} \mu dQ'_I(x)\Big] \tag{2.7}$$

Thus, we can view the total drain current I_D as consisting of two components I_{D1} and I_{D2}, where I_{D1} is due to the presence of drift alone and is given by

$$I_{D1} = \frac{W}{L}\int_{\psi_{s0}}^{\psi_{sL}} \mu[-Q'_I(x)]d\psi_s \tag{2.8}$$

and I_{D2} is due to the presence of diffusion alone and is given by

$$I_{D2} = \frac{W}{L}\phi_t \int_{Q'_{I,source}}^{Q'_{I,drain}} \mu dQ'_I(x) \tag{2.9}$$

$Q'_I(x)$ can be expressed in terms of ψ_s as [15]

$$Q'_I(x) = -C'_{ox}\Big(V_{GB} - V_{FB} - \psi_s(x) + \gamma\sqrt{\psi_s(x)}\Big) \tag{2.10}$$

where C'_{ox} ($= \epsilon_{ox}/t_{ox}$, with ϵ_{ox} being the oxide permittivity and t_{ox} the oxide thickness) is the oxide capacitance per unit area, V_{FB} is the flatband voltage, and γ ($= \sqrt{2q\epsilon_s N_A}/C'_{ox}$, where ϵ_s is silicon permittivity and N_A is the substrate doping concentration) is the body effect coefficient. Weak inversion is defined as the region of operation where the inversion charge Q'_I is negligible as compared to the depletion charge Q'_B. Thus, applying this definition of weak inversion to Eq.(2.10), we obtain the following relation for the surface potential ψ_s in weak inversion, which happens to be constant along the channel from source to drain [15]

$$\psi_s(V_{GB}) = \left(-\frac{\gamma}{2} + \left(\frac{\gamma^2}{4} + V_{GB} - V_{FB}\right)^{1/2}\right)^2 \tag{2.11}$$

Since the surface potential is constant from source to drain, hence, from Eq.(2.8), it can be seen that the drift current component will be zero. Therefore, the entire drain current is due to the diffusion component alone. In order to obtain this diffusion current component, Eq.(2.9) is rewritten as

$$I_D = I_{D2} = -\frac{W}{L}\mu\phi_t(Q'_{I,source} - Q'_{I,drain}) \tag{2.12}$$

where $Q'_{I,source}$ and $Q'_{I,drain}$ can be given by [15]

$$Q'_{I,source} = -\frac{\gamma C'_{ox}}{2[\psi_{s0}(V_{GB})]^{1/2}}\phi_t e^{[\psi_{s0}(V_{GB}) - 2\Phi_F - V_{SB}]/\phi_t} \tag{2.13}$$

and

$$Q'_{I,drain} = -\frac{\gamma C'_{ox}}{2[\psi_{sL}(V_{GB})]^{1/2}}\phi_t e^{[\psi_{sL}(V_{GB}) - 2\Phi_F - V_{DB}]/\phi_t} \tag{2.14}$$

where Φ_F is the bulk potential, given by

$$\Phi_F = \phi_t \, ln\frac{N_A}{n_i} \tag{2.15}$$

where n_i is the intrinsic carrier concentration, and V_{SB} and V_{DB} are the applied source-to-body and drain-to-body voltages respectively. Substituting Eqs.(2.13) and (2.14) in Eq.(2.12), and after some algebraic manipulation, we obtain [15]

$$I_D = \frac{W}{L} I'_X e^{\frac{V_{GS}-V_X}{n\phi_t}} \left(1 - e^{\frac{-V_{DS}}{\phi_t}}\right) \tag{2.16}$$

where [15]

$$V_X = V_{FB} + 1.5\Phi_F + \gamma(1.5\Phi_F + V_{SB})^{1/2} \tag{2.17}$$

$$I'_X = \mu C'_{ox} \phi_t^2 \frac{\gamma}{2(1.5\Phi_F + V_{SB})^{1/2}} e^{\frac{-0.5\Phi_F}{\phi_t}} \tag{2.18}$$

and the quantity n, defined as the subthreshold slope, is given by [15]

$$n = 1 + \frac{\gamma}{2(1.5\Phi_F + V_{SB})^{1/2}} \tag{2.19}$$

This current equation [Eq.(2.16)] is valid only in the weak inversion region, and the gate-to-source voltage (V_{GS}) range in which this equation is valid is given as [15]

$$V_L \leq V_{GS} \leq V_M \tag{2.20}$$

The term V_L is given by [15]

$$V_L = V_{FB} + \Phi_F + \gamma\sqrt{\Phi_F + V_{SB}} \tag{2.21}$$

and it is the applied gate-to-source voltage at which inversion just starts. In an actual MOS transistor, the observable (and usable) drain current is the sum of the channel current and a reverse junction leakage current (which includes the leakage of the source/drain-substrate n^+p junction as well as leakage across the depletion region under the channel). Thus, a pragmatic lower limit for weak inversion operation can be taken as the point where the leakage current can be neglected as compared to the channel current. The upper limit V_M is given as [15]

$$V_M = V_{FB} + 2\Phi_F + \gamma\sqrt{2\Phi_F + V_{SB}} \tag{2.22}$$

and it is defined as the gate-to-source voltage beyond which the MOS device enters the moderate inversion region of operation.

The above subthreshold current equation is a simplified equation suitable for hand calculations and also to understand the behavior of long channel devices qualitatively.

2.3 The Current Voltage Characteristics of an n-Channel MOSFET in Subthreshold

In this section, the current-voltage characteristics of an NMOS device are presented for four different situations. The important NMOS device parameters used for these simulations are $V_{TN} = 0.627\ V$, (W/L) = (25/1), $t_{ox} = 9.6$ nm, $\gamma = 0.793853\ V^{\frac{1}{2}}$, and $N_A = 1.7 \times 10^{17}\ cm^{-3}$. The simulations were done using the TANNER EDA [20] tool with 0.5 μm technology file supported by BSIM3v3 model [21].

1. **The I_D vs. V_{DS} characteristics with V_{GS} as a parameter, keeping V_{SB} constant:**

   Figure 2.2 shows these characteristics for $V_{SB} = 0\ V$, and $V_{GS} = 0.4$ V, 0.45 V, and 0.5 V. These curves can be explained as follows. If the applied value of V_{GS} is such that the NMOS device is in the subthreshold region of operation, then for small values of V_{DS}, the inversion layer will approximately be uniform in thickness from source to drain. As a result, the channel behaves as a linear resistor, and, thus, the drain current increases linearly for small values of V_{DS}. As V_{DS} increases and approaches $V_{DS,sat}$, the current starts to become almost independent of V_{DS}. This $V_{DS,sat}$ is defined as the drain-to-source saturation voltage in weak inversion, and is approximately given by $3kT/q$ [refer to Eq.(2.16)]. Thus, $V_{DS,sat}$ in weak inversion is independent of V_{GS}, and is considerably lower than the saturation voltage under strong inversion region of operation. This fact can be useful for low voltage applications, as lower drain-to-source voltage will be required to keep the MOS device in saturation. The positive slope of the characteristics beyond saturation is caused by the charge sharing and the drain induced barrier lowering (DIBL) effects.

2. **The I_D vs. V_{DS} characteristics with V_{SB} as a parameter, keeping V_{GS} constant:**

   Figure 2.3 shows these characterstics for $V_{GS} = 0.5$ V, and $V_{SB} = 0$ V, 0.05 V, and 0.1 V. For constant V_{GS}, increment in V_{SB} causes the depletion charge to increase, thereby reducing the inversion charge, which results in reduced drain current. Hence, I_D vs. V_{DS} curves shift downward with increasing V_{SB}.

3. **The I_D vs. V_{GS} characteristics for $V_{DS} < 3kT/q$, keeping V_{SB} constant:**

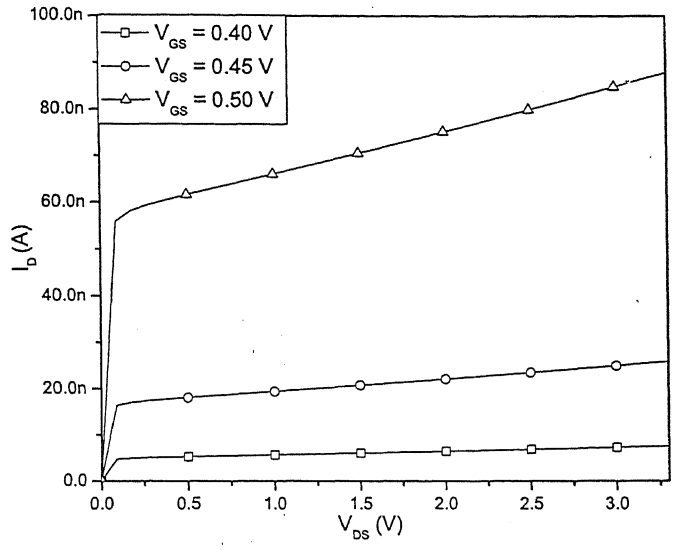

Figure 2.2. Plots of I_D vs. V_{DS} with V_{GS} as a parameter ($V_{SB} = 0\ V$).

Figure 2.4 shows these characteristics for $V_{SB} = 0$ V, and $V_{DS} = 30$ mV, 40 mV, and 50 mV. The dependence of I_D on V_{GS} is exponential as can be seen from Eq.(2.16). Thus, the I_D vs. V_{GS} characteristics will be exponential in nature for constant V_{SB}. For $V_{DS} < 3kT/q$, the channel behaves as a linear resistor, and, hence the I_D curves will shift upward with increasing V_{DS}.

4. **The I_D vs. V_{GS} characteristics for $V_{DS} > 3kT/q$, keeping V_{SB} constant:**

Figure 2.5 shows these characteristics for $V_{SB} = 0$ V, and $V_{DS} =$ 100 mV, 110 mV,and 120 mV. The I_D vs. V_{GS} characteristics will be exponential in nature for this case also, however, since V_{DS} is now greater than $V_{DS,sat}$, hence, I_D will have no dependence on V_{DS}, and all curves (for different V_{DS} values) would overlap on a single

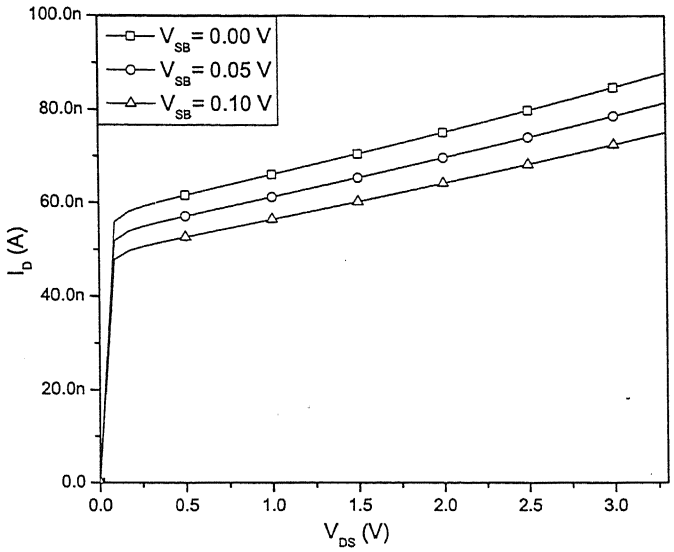

Figure 2.3. Plots of I_D vs. V_{DS} with V_{SB} as a parameter ($V_{GS} = 0.5\ V$).

characteristic, as is observed from Fig.2.5.

It is to be noted that the results presented here are for an NMOS device. For PMOS devices, the curves will be of similar nature but the current and voltage polarities will be opposite to that of the NMOS case. One should note here that the curves are qualitatively similar to their strong inversion counterparts, except the fact that the drain-to-source saturation voltage is independent of the gate-to-source voltage, and is given approximately by $3kT/q$, as is obvious from Eq.(2.16)

Based on the above discussion, it can be inferred that there is really no need to change the schematic of the design; just operating the devices in weak inversion region will be sufficient in most of the cases in order to achieve lower power dissipation. However, on the other hand, operation of the circuits in the subthreshold region affects some critical circuit performance parameters negatively, e.g., if an op-amp is operated in the subthreshold region, its slew

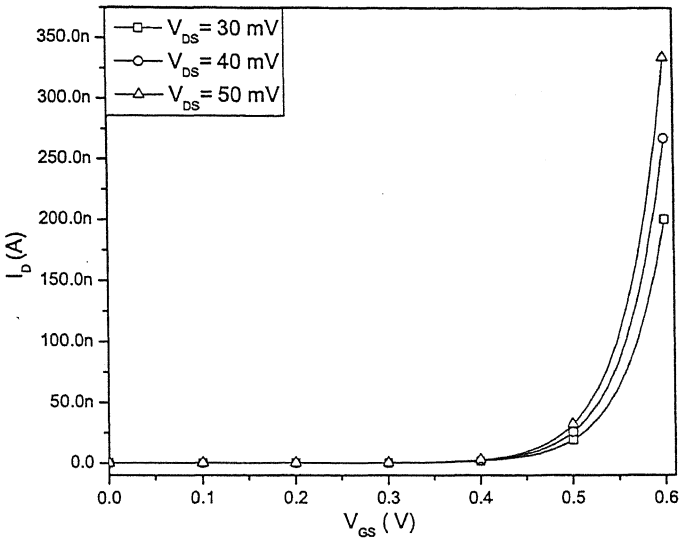

Figure 2.4. Plots of I_D vs. V_{GS} for $V_{DS} < 3kT/q$ ($V_{SB} = 0\ V$).

rate and frequency response will be very poor as compared to its operation in the strong inversion region. Hence, in order to achieve improvement in these areas also, one may need to use some new auxiliary circuits. In the next section, the small-signal model for an n-channel MOSFET in saturation under weak inversion is discussed.

2.4 Small Signal Model for Saturation Region Under Weak Inversion

For hand calculation, the complete small-signal model, as shown in Fig.2.6, can be used. The parameters shown in this figure are described as follows. The small-signal transconductance g_m is given by [15]

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{1}{n}\frac{I_D}{\phi_t} \tag{2.23}$$

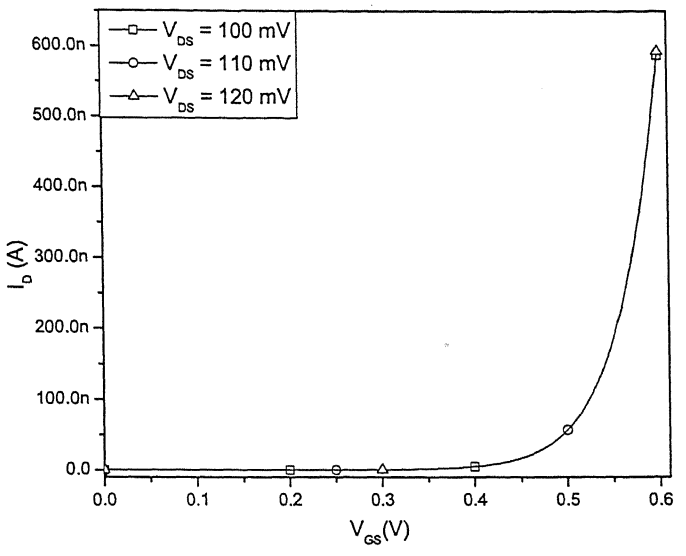

Figure 2.5. Plots of I_D vs. V_{GS} for $V_{DS} > 3kT/q$ ($V_{SB} = 0\ V$).

The small-signal substrate transconductance g_{mb} is given by [15]

$$g_{mb} = \frac{\partial I_D}{\partial V_{SB}} = \frac{n-1}{n}\frac{I_D}{\phi_t} \tag{2.24}$$

and the output resistance r_d is given as [15]

$$r_d = \frac{\partial V_{DS}}{\partial I_D} = \frac{1 - e^{\frac{-V_{DS}}{\phi_t}}}{e^{\frac{-V_{DS}}{\phi_t}}}\frac{\phi_t}{I_D} \tag{2.25}$$

This equation predicts that r_d rapidly diverges to infinity with increasing V_{DS}. However, this neglects the direct influence of the drain field on the channel. The charge sharing and the DIBL effects cause the effective threshold voltage of the device to decrease with increasing V_{DS}. Hence, the current increases with V_{DS}. Thus, a behavior similar to that for strong inversion is exhibited,

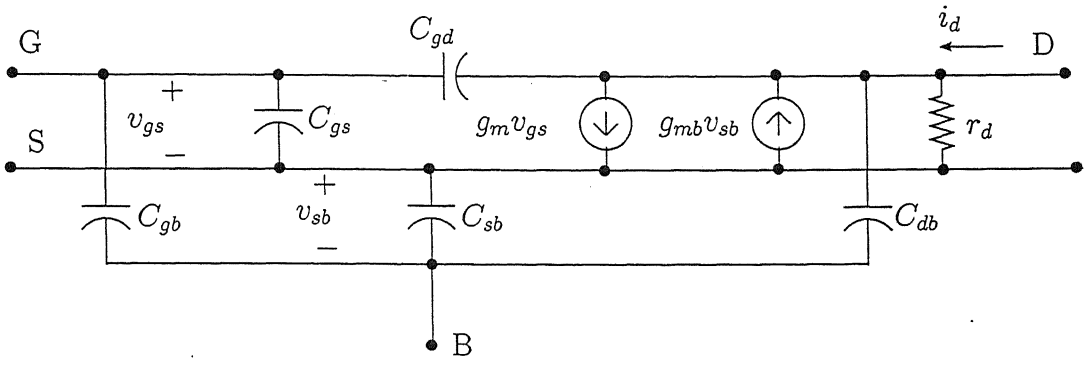

Figure 2.6. The small-signal model of an NMOS device under weak inversion.

hence, r_d can be given as

$$r_d = \frac{V_{AW}}{I_D} \tag{2.26}$$

where V_{AW} is the magnitude of the intercept of I_D at the negative V_{DS} axis, when the drain current characteristics curves are extended from a point in the saturation region of the weak inversion region of operation. Thus, V_{AW} plays the same role which V_A ($\simeq 1/\lambda$, where λ is the channel length modulation parameter) plays in strong inversion, and $V_{DS} > 3\phi_t$ has been imposed as the condition to ensure operation in the almost flat part of the I_D vs. V_{DS} characteristic [15].

2.5 Capacitances in Weak Inversion

In weak inversion, the charge contained in the inversion layer is negligible as compared to the depletion charge throughout the length of the channel, and the gate "sees" the depletion region directly through the oxide. A small increase in V_{GB} will cause some charges to enter through the substrate terminal and this will be balanced by some gate charge leaving through the gate terminal. Hence, there exists a capacitance (C_{gb}) between the gate and the substrate, which is given as [15]

$$C_{gb} = C_{ox}\frac{\gamma}{2\sqrt{\frac{\gamma^2}{4} + V_{GB} - V_{FB}}} \tag{2.27}$$

where C_{ox} $(= C'_{ox}WL)$ is the total oxide capacitance. Varying V_{SB} or V_{DB} in weak inversion can vary the inversion charge drastically in relative sense, however, the amount of this charge remains negligible as compared to the gate charge and the bulk depletion charge. Hence, the gate and the substrate do not feel the variation of V_{SB} and V_{DB}, that is why the capacitances associated with gate-to-source (C_{gs}), drain-to-substrate (C_{db}), source-to-substrate (C_{sb}), and gate-to-drain (C_{gd}) are all approximately equal to zero [15], i.e.,

$$C_{gs} \approx C_{db} \approx C_{sb} \approx C_{gd} \approx 0 \tag{2.28}$$

Thus, the overall capacitance of a MOSFET operating under weak inversion is quite small. However, looking at these low capacitances, one can not conclude that the circuit will be useful for high speed applications. On the contrary, circuits in weak inversion are quite sluggish because of the very low amount of available charging and discharging current.

Being equipped with the knowledge of the current-voltage characteristics as well as the small-signal model for n and p-channel MOSFETs in the weak inversion region of operation, the behavior of the circuits operating in this region can be better understood. The next chapter describes some examples of circuits operating under weak inversion along with their relative merits and demerits.

Chapter 3

Subthreshold Region of Operation of Differential Amplifiers: Advantages and Limitations

3.1 Introduction

In this chapter, the design aspects of a differential amplifier (DA) that requires minimum power are considered. The advantages and limitations of operation in the subthreshold region are discussed. Existing techniques that overcome the slew rate limitation of DAs are also explained.

3.2 Single Stage Differential Amplifier in The Subthreshold Region of Operation

The DA shown in Fig.3.1 is biased in the subthreshold region of operation. M_1 and M_2 form the input transconductance stage, and the current mirror M_3-M_4 is used as the load to the amplifier. The current mirror M_5-M_6 is

used to bias the DA. The constant current source I_{BIAS} is used to generate a constant bias current I_{SS} for the DA. In order to bias the DA in the subthreshold region of operation, the biasing current I_{SS} is chosen to be

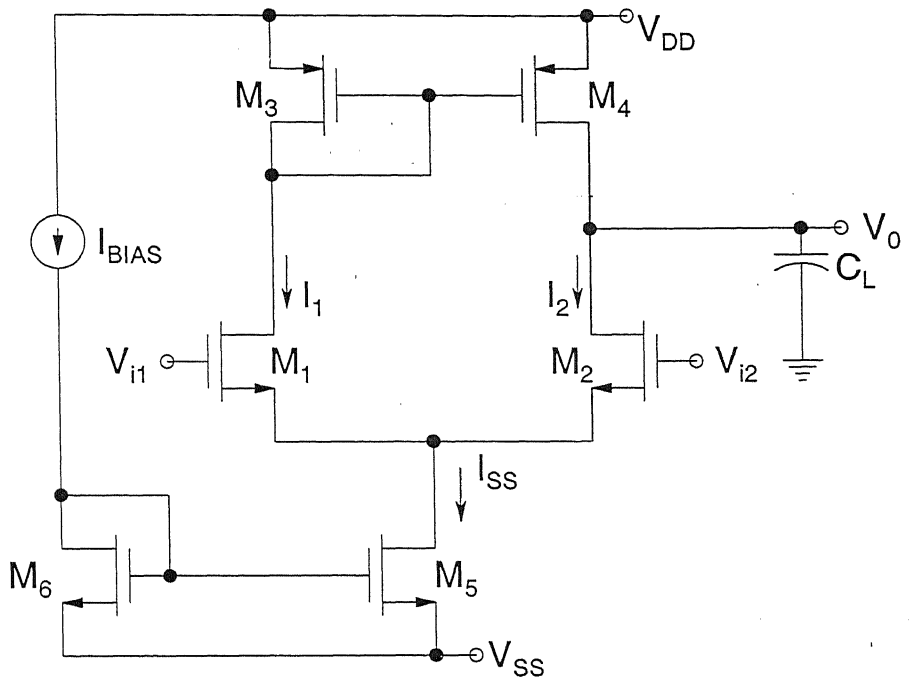

Figure 3.1. A simple actively loaded and actively biased DA, biased in the subthreshold region of operation, and driving a capacitive load.

sufficiently low. Using the small-signal model given in Section 2.3, the critical circuit performance parameters of the DA can be obtained. The small-signal low frequency voltage gain A_{vo} [$= v_0/(v_{i1}-v_{i2})$, where v_0, v_{i1}, and v_{i2} are small-signal components of V_o, V_{i1}, & V_{i2} respectively] of this amplifier can be given by

$$A_{vo} = g_{m2}\frac{r_{d2}r_{d4}}{r_{d2}+r_{d4}} \tag{3.1}$$

where g_m is the transconductance and r_d is the output resistance of the MOS

device. Substituting the expression for g_m and r_d from Eqs.(2.23) and (2.25) respectively in Eq.(3.1), we obtain

$$A_{vo} = \frac{1}{n_2 \phi_t} \frac{V_{AW2} V_{AW4}}{V_{AW2} + V_{AW4}} \tag{3.2}$$

where V_{AW} is given by Eq.(2.26), and n_2 is given by Eq.(2.19). The gain-bandwidth product (GBP) of the amplifier is given by

$$GBP = \frac{g_{m2}}{C_L} = \frac{I_2}{\phi_t} \frac{1}{C_L} \tag{3.3}$$

where C_L is the capacitance associated with the output node and I_2 is the drain current of M_2.

It is interesting to note from Eq.(3.2) that the gain of the op-amp is independent of I_1 and I_2, where I_1 is the drain current of M_1. The dynamic performance of an operational amplifier is dependent on the GBP and the slew rate of the amplifier. The GBP of the amplifier is low due to the lower value of the available biasing current, as is obvious from Eq.(3.3). In order to improve the dynamic performance, the slew rate of the DA should be high, which is a large signal phenomenon, affecting the settling time of the circuits. The next section discusses the reasons behind this slew rate limitation and the ways to improve it.

3.3 Slew Rate Limitation of the Differential Amplifier

Consider the DA driving a load capacitance C_L, as shown in Fig.3.1, with V_{i2} grounded. If a step input is applied to V_{i1} that goes from 0 to V_{SS}, then M_1, M_3, and M_4 cut off, and the total bias current I_{SS} flows from C_L through M_2/M_5 to V_{SS}. Under these conditions, C_L is discharged at its maximum

rate, called the negative slew rate. This rate of discharge, assuming that C_L includes all the capacitances associated to the output node of the DA, is given by

$$\frac{dV}{dt} = \frac{I_{SS}}{C_L} \tag{3.4}$$

It can also be seen that if a positive step pulse going from 0 to V_{DD} is applied to the input V_{i1}, then M_2 will turn off and the current through M_1, M_3, and M_4 would be I_{SS}. Therefore, the maximum rate at which the load capacitance can be charged is given by Eq.(3.4) as well, and this gives the positive slew rate. Hence from Eq.(3.4), it is obvious that if the DA is operating in the weak inversion region, then the biasing current I_{SS} will be considerably low, and, thus, the slew rate of the DA will also be very low.

In MOS amplifiers, the slew rate can easily be improved by increasing I_{SS}, achieved by operating the input transistors in strong inversion. However, this solution is not satisfactory for low power applications, where one wants to have the maximum GBP with the minimum possible biasing current. The slew rate limitation for operation under weak inversion is caused by the fact that the current available to bias the DA is limited. The slew rate can thus be improved by using a current source, the magnitude of which increases as the input differential signal becomes large; this concept is reffered to in literature as adaptive biasing.

3.4 The Concept of Adaptive Biasing

Adaptive biasing can reduce the power dissipation in an amplifier, while at the same time increase the output current drive capability. Figure 3.2 illustrates this idea. I_{SS} is a constant current source, the magnitude of which is independent of V_{i1} and V_{i2}, while the functioning of I_{SS1} and I_{SS2} is as follows: when V_{i1} and V_{i2} are equal, the current carried by the current

sources I_{SS1} and I_{SS2} are zero (i.e., they behave as open circuits). The DA dc bias current is then simply I_{SS}, the same as that an ordinarily biased DA would have. If now V_{i1} becomes greater than V_{i2}, then the current carried by

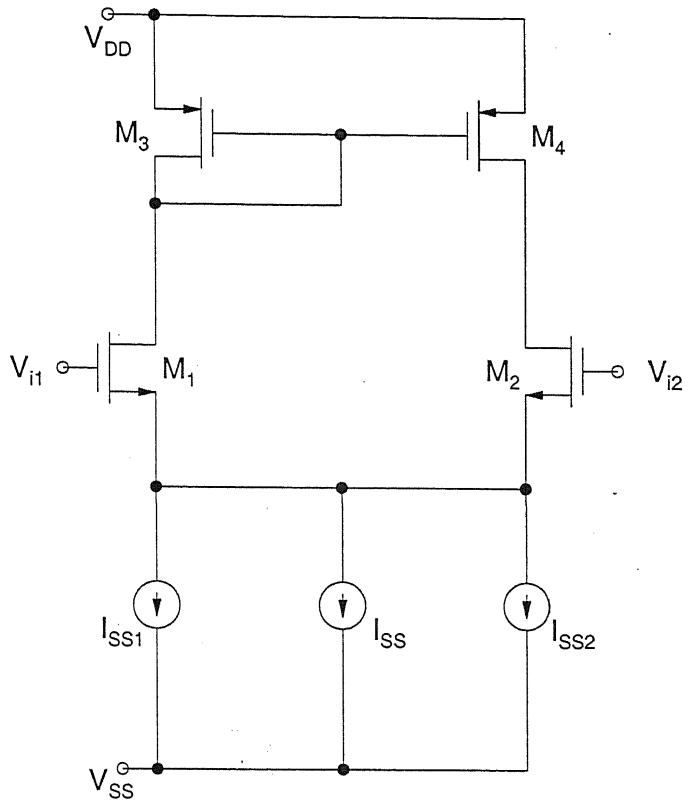

Figure 3.2. The concept of adaptive biasing [16].

the current source I_{SS1} increases above zero, effectively increasing the dc bias current of the DA. Similarly, if V_{i2} becomes larger than V_{i1}, the current carried by the current source I_{SS2} increases above zero. The DA output current is generally limited to I_{SS} when one side of the DA cuts off. However, now the maximum output current that can be delivered to the output capacitance is either $I_{SS} + I_{SS1}$ or $I_{SS} + I_{SS2}$, depending on the relative magnitudes of V_{i1}

and V_{i2}. Thus, the slew rate limitation problem of the DAs can be reduced to some extent by using adaptive biasing techniques.

In order to improve the dynamic or transient performance of the amplifiers, the concept of adaptive biasing was first introduced by Degrauwe et al. [10]. Since then, many techniques have been suggested in the literature to realize adaptive biasing [8-14]. Following are the two most popular techniques among these. Figure 3.3 is an adaptively biased input stage of an OTA [10].

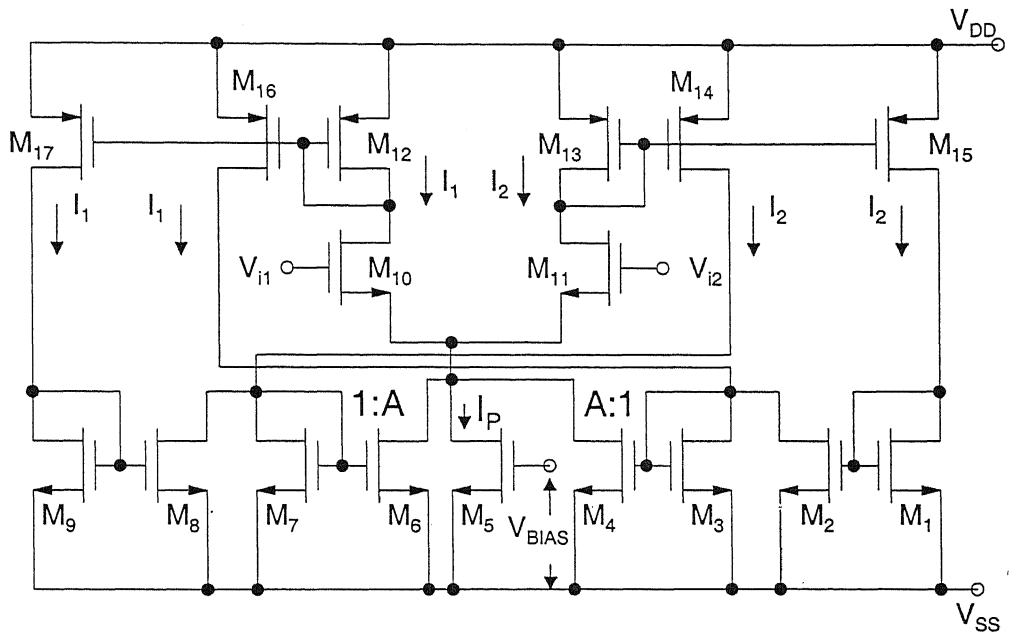

Figure 3.3. The schematic of an adaptively biased OTA input stage [10].

The OTAs are basically unbuffered op-amps. The working principle of the circuit given in Fig.3.3 is as follows. When a voltage is applied across the

input terminals of the OTA, the currents I_1 and I_2 become different. The bias current of the amplifier is made dependent on the input differential voltage by adding an additional current source to the main bias current source, which realizes the function $A|I_1 - I_2|$, where A is called the current feedback factor. This additional current source is realized by two current subtractors, the schematic of which is shown in Fig.3.4. The working principle of this current

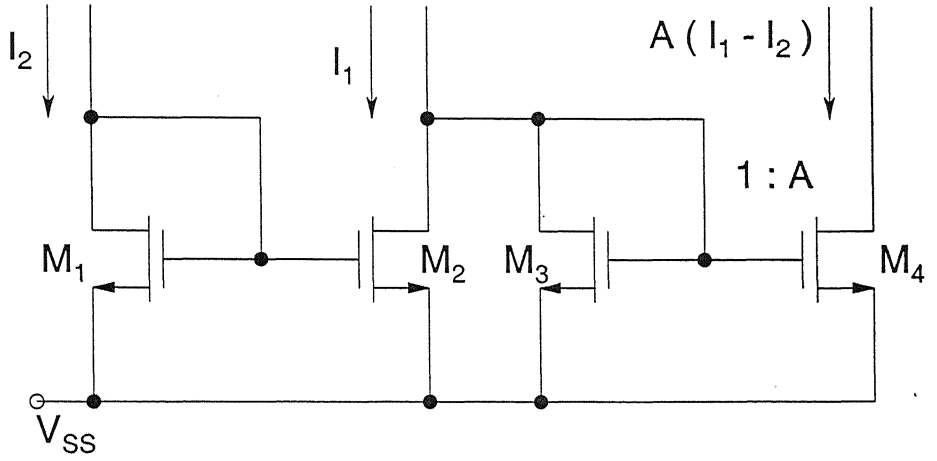

Figure 3.4. The schematic of a current subtractor [10].

subtractor is as follows. If the currents I_1 and I_2 are equal, then zero current flows in M_3 and M_4. Also, if I_2 is greater than I_1, then also zero current flows in M_3 and M_4. However, if I_1 is grater than I_2, then the difference between these two currents, i.e., $(I_1 - I_2)$ flows in M_3. Since M_4 is A times wider than M_3, a current equal to $A(I_1 - I_2)$ flows in M_4. By putting the subtractors in the scheme of the simple OTA, where the current at the inputs of the subtractors are provided by means of current mirrors, we obtain the circuit

shown in Fig.3.3. If both inputs of the amplifier are equal to each other, then the currents I_1 and I_2 will also be equal to each other, and the total bias current is thus simply I_P. Only when there is difference between the two input signals, the total bias current will be $I_P + A|I_1 - I_2|$, and this increased bias current will reduce the charging and discharging times of the capacitance associated with the output node. However, one thing worth noting from power dissipation point of view is that, in quiescent condition (i.e., when $V_{i1} = V_{i2}$), there will be an additional power equal to $2I_P(V_{DD} - V_{SS})$, as compared to the conventional OTA. Thus, the stand-by power dissipation of this adaptive biasing circuit is considerable.

The other technique presented here has been proposed by Baswa et al. [11], the schematic of which is shown in Fig.3.5. The working principle of this circuit is as follows. At the non-inverting input of the NMOS DA, the common-mode sensing circuit produces a voltage proportional to the common-mode input signal plus some dc voltage (this dc offset voltage appears at the output of the common-mode sensing circuit for zero value of common-mode input voltage). The inverting terminal of the NMOS DA is connected to the common source point of the PMOS DA. When a differential input signal is applied, the voltage at the common source point will rise and this voltage will be compared with the common mode voltage (produced by the common mode sensing circuit) by the NMOS DA. Thus, a voltage output, proportional to the difference at the inputs of the NMOS DA, will be produced. This output voltage is used to bias the PMOS DA. Hence, the bias current is made dependent on the applied input voltages. Thus, a large biasing current will be available for a large differential input signal, thereby making the circuit faster. The drawback of this technique is that the common mode sensing circuit as well as the NMOS DA requires considerable amount of quiescent power. Therefore, both the techniques described here require additional quiescent current sources, thus, making the standby power dissipation of the circuits considerable.

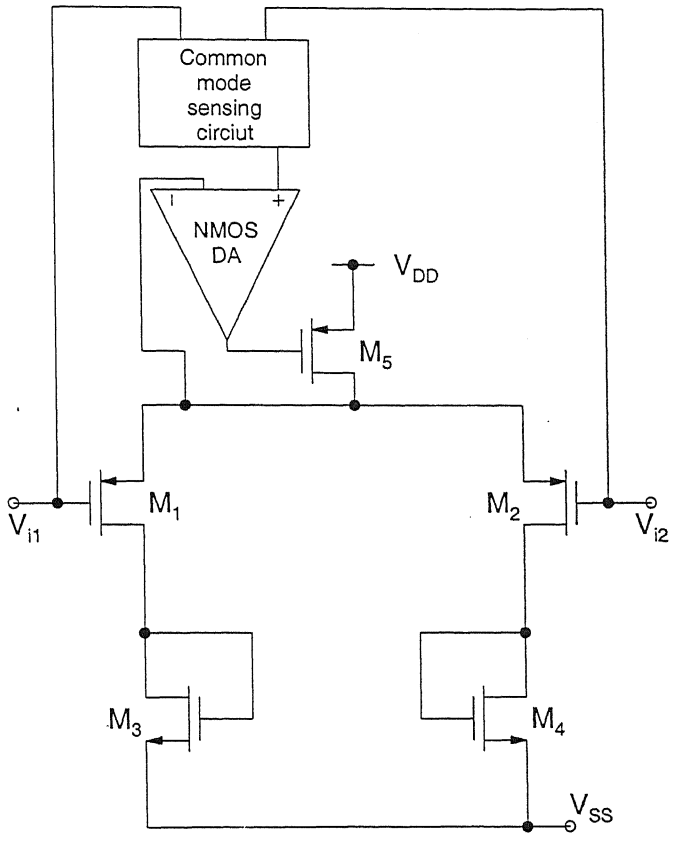

Figure 3.5. The schematic of an OTA input stage with adaptive biasing [11].

In modern applications, very stringent requirements are imposed on adaptive biasing circuits, some of which are as follows;

- ➢ Ability to set low and accurately controlled quiescent currents.
- ➢ Large current sourcing capability.
- ➢ Low voltage operation.
- ➢ Reduced number of transistors to limit noise, increase bandwidth, and reduce silicon area requirements.

The adaptive biasing circuit which satisfies all these requirements will be the best suited for low-voltage low-power applications. In the next chapter, an adaptive biasing block has been proposed in this work here, which satisfies these constraints to a lrage extent.

Chapter 4

Improvement in the Dynamic Performance of an OTA Using the Proposed Adaptive Biasing Circuit

4.1 Introduction

In this chapter, a new adaptive biasing circuit for differential amplifiers is proposed. Operation of this circuit is explained and simulation results are also discussed. The proposed circuit has been used in an Operational Transconductance Amplifier (OTA) and it has been shown that it improves the dynamic performance of the OTA without affecting other circuit performance parameters adversely.

4.2 Working Principle of the Proposed Adaptive Biasing Circuit

The schematic of the adaptive biasing circuit proposed in this work here is shown in Fig. 4.1. Transistors M_1-M_4 form the core of the proposed circuit. The gates of these transistors are cross coupled and V_1 and V_2 are the inputs to the adaptive biasing circuit. Transistors M_5 and M_6 are acting as simple current sources, gates of which are connected to the drains of M_2 and M_4 respectively. The current mirror M_7-M_8 is used to add up the currents of transistors M_5 and M_6. In order to get sufficient current amplification, an additional current mirror M_9-M_{10} is used. This current mirror may not be required in cases where high current drive is not required. Since transistors M_1-M_4 have equal W/L ratios, hence, when the voltages at the gates of M_1 and M_2 are equal, the gate-to-source voltage of the lower transistor M_2 will be higher as compared to the gate-to-source voltage of the upper transistor M_1. However, since both of these transistors are connected in series, hence, the current through both of them must be the same. This is possible only if M_2 goes into the triode mode of the weak inversion region. Thus, in this case, the voltage at the gate of M_5 will be very close to the negative power supply V_{SS}. The same statement is true for the case of M_3-M_4 combination.

Now, even when the voltages at the gates of the upper transistors M_1 and M_3 are less than the voltages at the gates of the lower transistors M_2 and M_4 respectively, even then the lower transistors will remain in the triode region of weak inversion. In this case also, the gate voltages of transistors M_5 and M_6 $\left[V_G(M_5) \text{ and } V_G(M_6) \text{ respectively}\right]$ will be very close to V_{SS}.

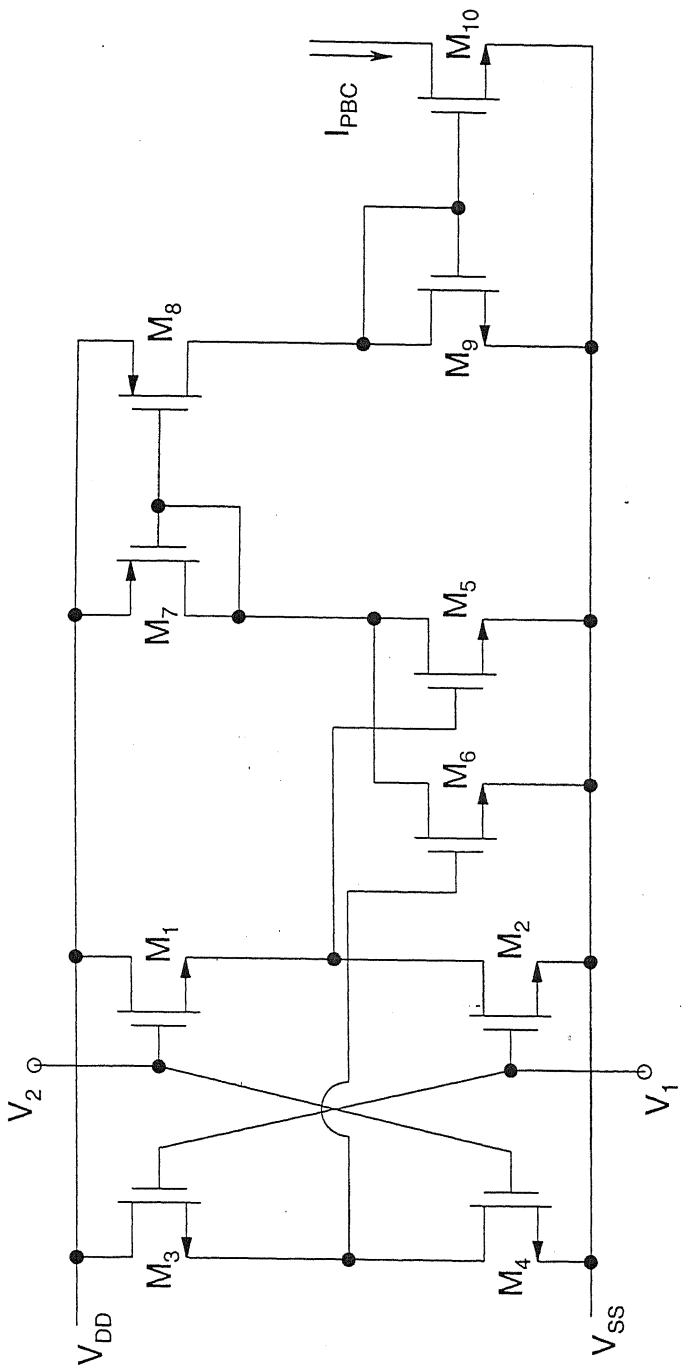

Figure 4.1. The schematic of the proposed adaptive biasing circuit.

Thus,

$$V_G(M_5) \approx V_{SS} \quad for \;\; V_2 \leq V_1 \tag{4.1}$$

As we start increasing the voltage at the gate of the upper transistor (M_1 or M_3) as compared to the gate voltage of the lower transistors (M_2 or M_4 respectively), the lower transistor comes out of the triode region and both upper as well as lower transistors will now be operating in the saturation mode of the weak inversion or strong inversion region, depending upon the magnitude of the supply voltages used. Thus, in this case from

$$I_{D1} = I_{D2} \tag{4.2}$$

where I_{D1} and I_{D2} are the drain currents of M_1 and M_2 respectively, we get

$$V_{GS1} = V_{GS2} \tag{4.3}$$

and, thus,

$$V_G(M_5) = (V_2 - V_1) + V_{SS} \tag{4.4}$$

Therefore, Eqns.(4.1) and (4.4) can be collectively written as

$$V_G(M_5) = \left\{ \begin{array}{ll} \approx V_{SS} & for \;\; V_2 \leq V_1 \\ (V_2 - V_1) + V_{SS} & for \;\; V_2 \geq V_1 \end{array} \right\} \tag{4.5}$$

Similarly,

$$V_G(M_6) = \left\{ \begin{array}{ll} \approx V_{SS} & for \;\; V_1 \leq V_2 \\ (V_1 - V_2) + V_{SS} & for \;\; V_1 \geq V_2 \end{array} \right\} \tag{4.6}$$

Transistor M_5 remains in the subthreshold region of operation as long as $(V_2 - V_1) \leq V_{TN}$, where V_{TN} is the threshold voltage of the NMOS devices.

Similarly, transistor M_6 remains in the subthreshold region of operation as long as $(V_1 - V_2) \leq V_{TN}$. When the gate voltages of M_5 and M_6 are close to V_{SS}, none of them is conducting as their gate-to-source voltages are not sufficient for them to conduct. When the gate voltages of M_5 and M_6 vary proportionately to the difference of the input signals, the current flow through these devices will also be dependent upon the differential input voltage. Now using current mirrors, these currents are summed up and amplified subsequently and can be used to bias any DA or OTA adaptively. If V_1 and V_2 are the inputs of the DA or OTA, then use of this circuit to bias the DAs and OTAs will give a bias current that is dependent upon the differential input signal. Thus, the drain current for M_7 can be given by

$$I_D(M_7) = \left\{ \begin{array}{ll} I_D(M_6) & for\ V_1 > V_2 \\ I_D(M_5) & for\ V_1 < V_2 \\ \approx 0 & for\ V_1 \approx V_2 \end{array} \right\} \tag{4.7}$$

Transistors M_5 and M_6 are assumed to be identical. Thus, from the subthreshold current equation [Eqn.(2.16)] in the saturation region, the current in M_7 can also be written as

$$I_D(M_7) = \left\{ \begin{array}{ll} \left(\frac{W}{L}\right)_5 I'_X exp\left(\frac{|V_1 - V_2| - V_X}{n\phi_t}\right) & for\ V_1 \neq V_2 \\ \approx 0 & for\ V_1 \approx V_2 \end{array} \right\} \tag{4.8}$$

where all the notations in Eq.(4.8) have already been defined before in Chapter 2. If M_7 and M_8 have W/L ratio given by 1:A_1, then

$$I_D(M_8) = I_D(M_9) = A_1 I_D(M_7) \tag{4.9}$$

Similarly, if M_9 and M_{10} have W/L ratio given by 1:A_2, then

$$I_D(M_{10}) = A_2 I_D(M_9) = I_{PBC} \tag{4.10}$$

This biasing circuit is used to bias the input differential stage of the op-amp as shown in Fig.4.2, where I_{PBC} is the current provided by the proposed biasing

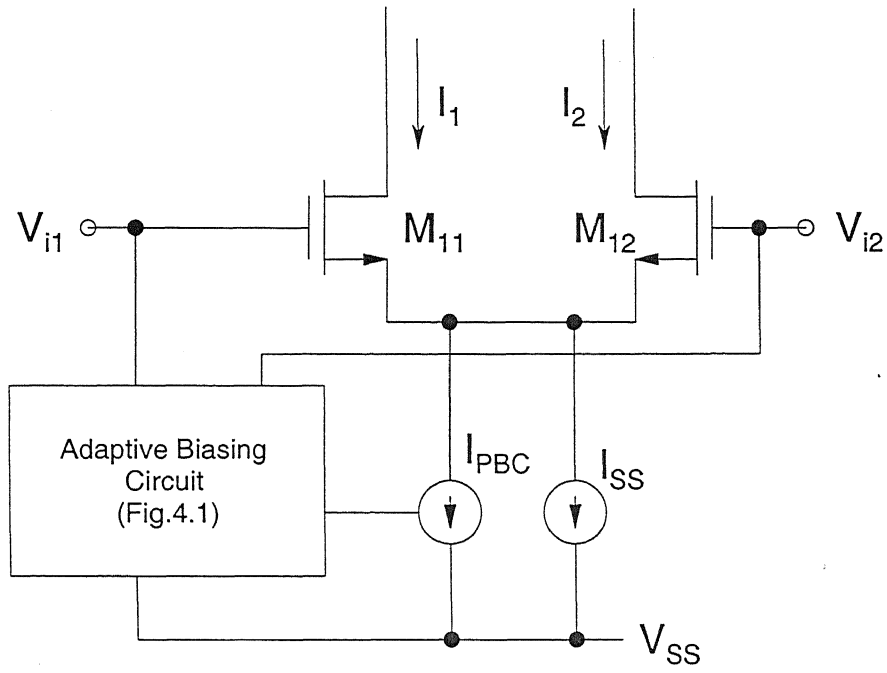

Figure 4.2. The schematic of an adaptively biased op-amp input stage using the proposed adaptive biasing circuit.

circuit and V_{i1} and V_{i2} are connected to V_1 and V_2 of the proposed adaptive biasing circuit respectively. The current source I_{SS} provides constant biasing current to the DA as in the case of an ordinarily biased op-amp. By using the previously developed current relation [Eq.(2.16)] between I_1 and I_2, given by

$$I_1 = I_2 \, exp\Big(\frac{V_1 - V_2}{n\phi_t}\Big) \tag{4.11}$$

Kirchhoff's current law will give us

$$I_{SS} + I_{PBC} = I_1 + I_2 \tag{4.12}$$

For $V_1 = V_2$, we know from Eq.(4.7) that $I_{PBC} = 0$ and from Eq.(4.11) we have $I_1 = I_2$, hence,

$$I_{SS}/2 = I_1 = I_2 \tag{4.13}$$

This is the case which is the same as that without the proposed adaptive biasing circuit. Now when $V_1 \neq V_2$, I_{PBC} will have some non-zero value [from Eq.(4.8)], and from Eq.(4.12), we have

$$I_{SS} + A_1 A_2 \left(\frac{W}{L}\right)_5 I'_X \; exp\left(\frac{|V_1 - V_2| - V_X}{n\phi_t}\right) = I_1 + I_2 \tag{4.14}$$

Thus, in this case, the total bias current of the DA has been increased which should improve the slew rate. Using Eqn.(4.11) in Eqn.(4.14), the current I_2 can be given as

$$I_2 = \frac{I_{SS} + A_1 A_2 \left(\frac{W}{L}\right)_5 I'_X \; exp\left(\frac{|V_1 - V_2| - V_X}{n\phi_t}\right)}{1 + \; exp\left(\frac{V_1 - V_2}{n\phi_t}\right)} \tag{4.15}$$

Similarly, I_1 can be obtained as

$$I_1 = \frac{I_{SS} + A_1 A_2 \left(\frac{W}{L}\right)_5 I'_X \; exp\left(\frac{|V_1 - V_2| - V_X}{n\phi_t}\right)}{1 + \; exp\left(\frac{V_1 - V_2}{n\phi_t}\right)} exp\left(\frac{V_1 - V_2}{n\phi_t}\right) \tag{4.16}$$

Hence, the currents are dependent on the differential input voltage, and for a large differential input voltage, the total biasing current becomes large, thus improving the slew rate.

4.3 Simulation Results

The TANNER EDA tool [20] has been used for all the simulations with 0.5 μm technology file supported by BSISM3v3 model [21]. The supply voltages (V_{DD} and V_{SS}) used are $\pm$1 V. Hence, MOSFETs of the adaptive biasing block can enter the strong inversion region of operation, depending upon the magnitudes of V_1 and V_2. Table 4.1 shows the W/L ratios of the devices used in the adaptive biasing block shown in Fig.4.1. When V_2 is

Table 4.1. W/L ratios of the devices used in the proposed adaptive biasing block shown in Fig.4.1.

Transistor Name	W/L Ratios (μm/μm)
M_1, M_2, M_3, M_4	1/25
M_5, M_6	25/1
M_7, M_8	1/1
M_9, M_{10}	30/1, 300/1

varied from +1 V to −1 V keeping $V_1 = 0$, the gate-to-source voltages of transistors M_5 and M_6 vary as described in Section 4.2. Figure 4.3 shows the voltage variations at the gates of transistors M_5 and M_6 as a function of the input differential voltage ($V_1 - V_2$). Figure 4.4 shows the plot of I_{PBC} as a function of the differential input voltage within a range of $\pm$1 V. The same plot is magnified within the range of $\pm$0.5 V and $\pm$0.3 V and are shown in Figs.4.5 and 4.6 respectively. It can be seen from these figures that I_{PBC} is a strong function of the differential input voltage and as the gate-to-source voltage of M_5 or M_6 starts to increase the current provied by these transistors will also increase drastically. At any given time, either M_5 or M_6 will conduct depending upon the relative magnitudes of the voltages at the two inputs. The currents of M_5 or M_6 will flow through M_7 and then amplified version of this current will be obtained at the drain of M_{10}.

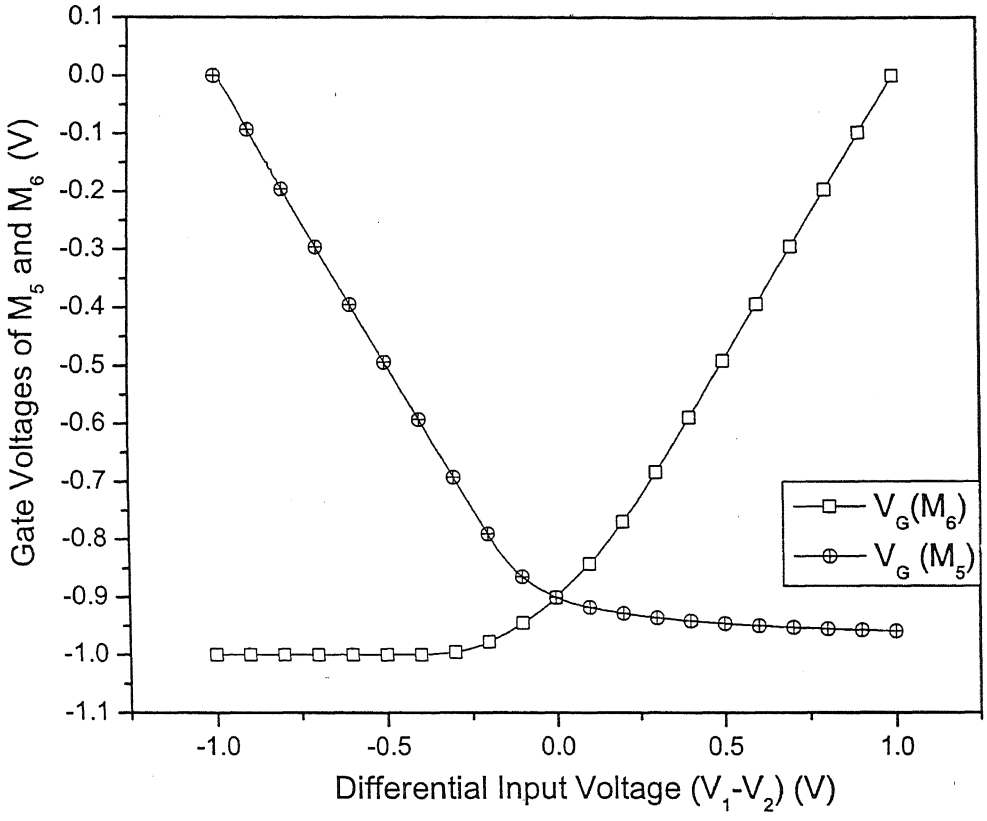

Figure 4.3. The variation of the gate voltages of M_5 and M_6 as a function of the differential input voltage.

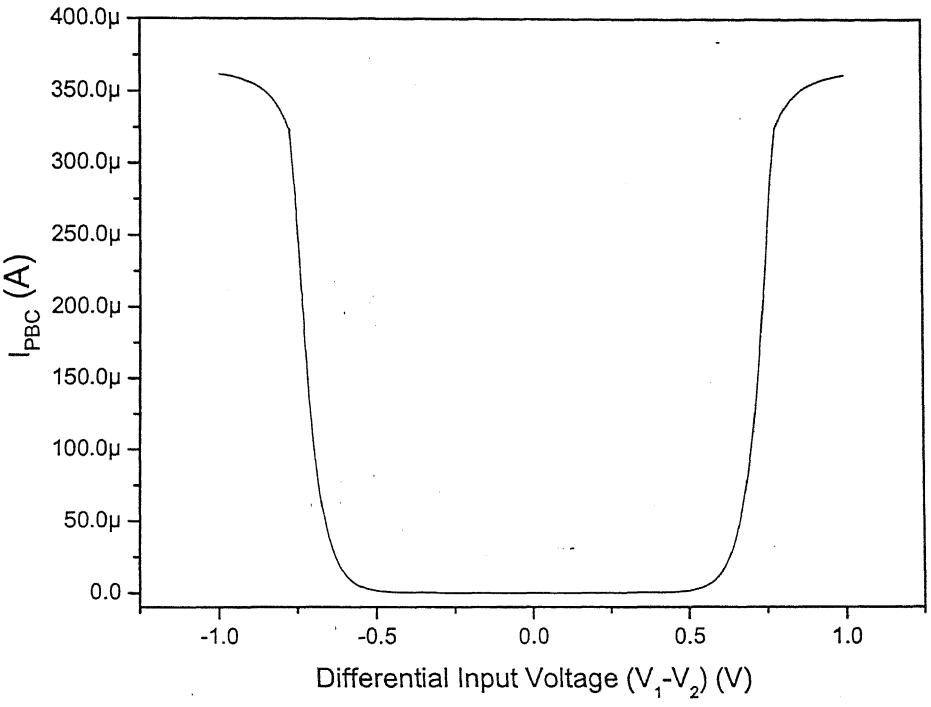

Figure 4.4. The output current I_{PBC} of the proposed adaptive biasing block as a function of the differential input voltage within a range of ± 1 V.

Figure 4.7 shows a conventional OTA [22] with local common mode feedback resistances R_1 and R_2 and without any adaptive biasing, and Fig.4.8 shows the same OTA but now with the proposed adaptive biasing block included. The W/L ratios of the MOSFETs used in the OTA are given in Table 4.2. The current mirror M_9-M_{10} is not used, instead the W/L ratio of M_8 has been changed to 300/1. The local common mode feedback resistances R_1 and R_2 are used to enhance the slew rate and the bandwidth of the OTA [22]. These resistances are taken to be equal to 10 kΩ for the simulation.The OTAs of Figs.4.7 and 4.8 are biased in the subthreshold region of operation with a constant current source of 5 μA, which is controlled by

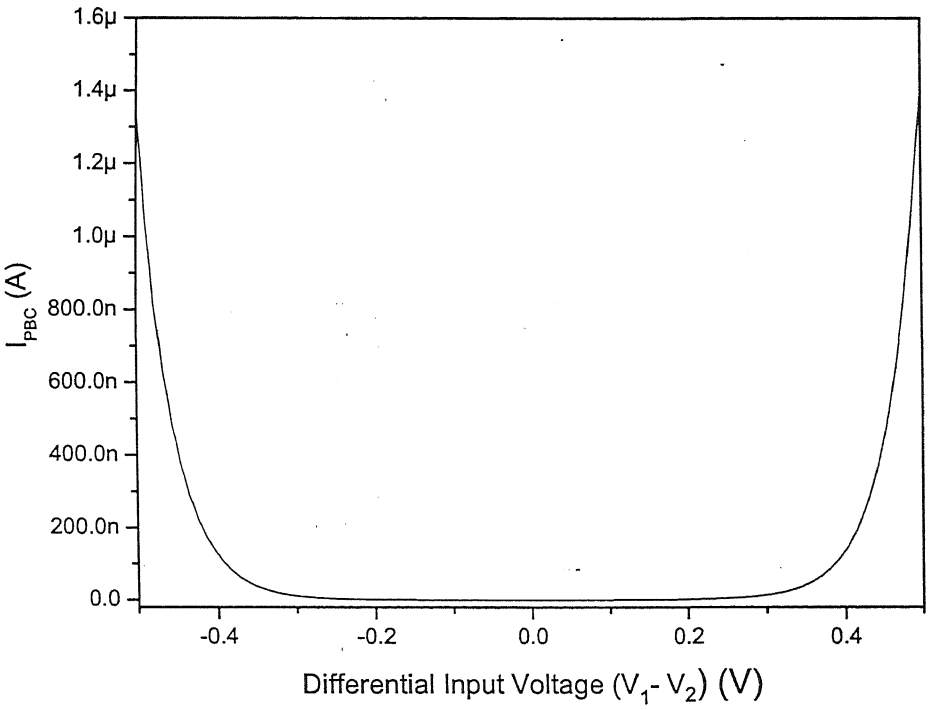

Figure 4.5. The output current I_{PBC} of the proposed adaptive biasing block as a function of the differential input voltage within a range of ± 0.5 V.

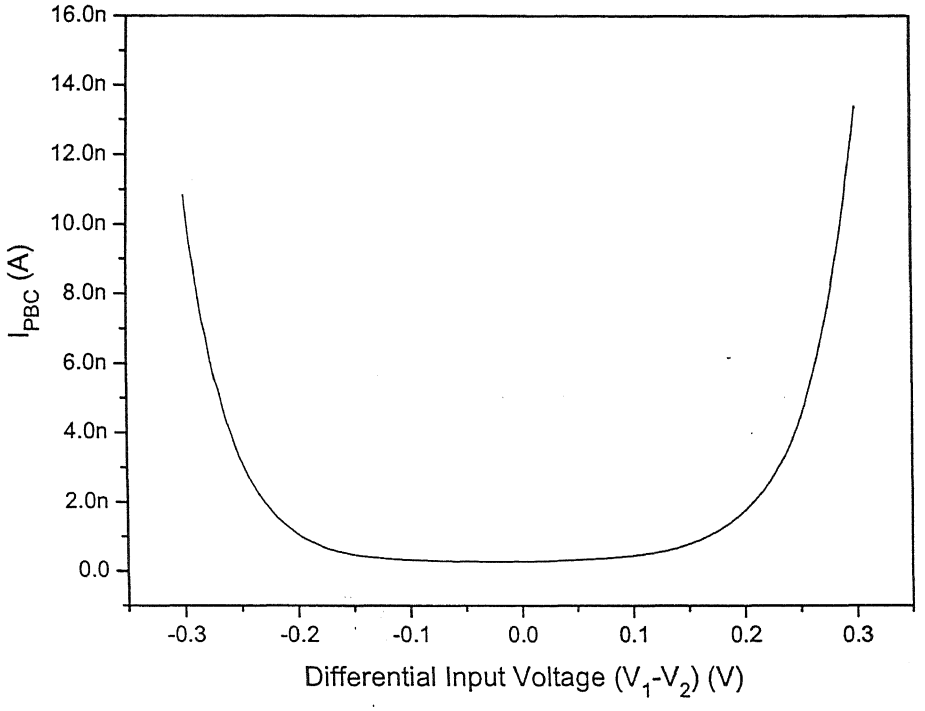

Figure 4.6. The output current I_{PBC} of the proposed adaptive biasing block as a function of differential input voltage within a range of ± 0.3 V.

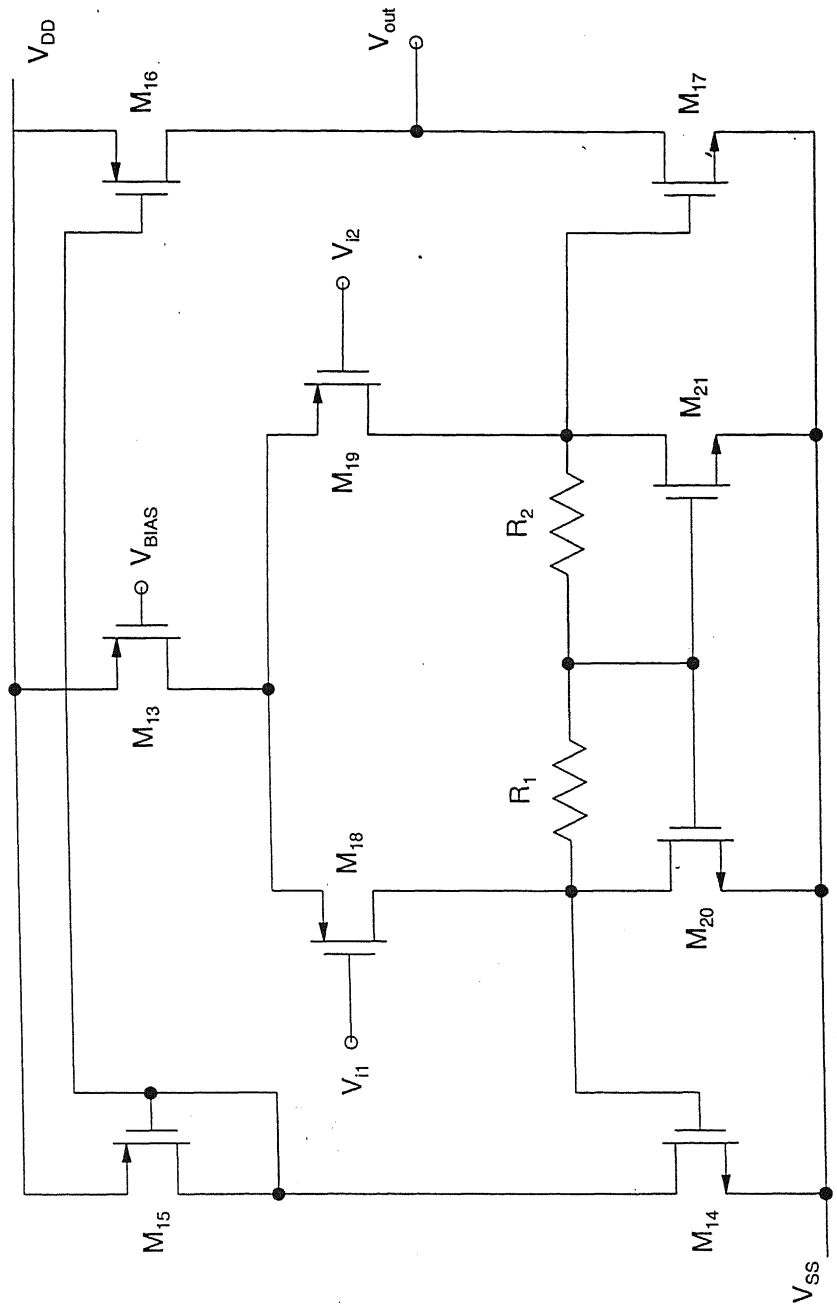

Figure 4.7. The schematic of an OTA without any adaptive biasing [22].

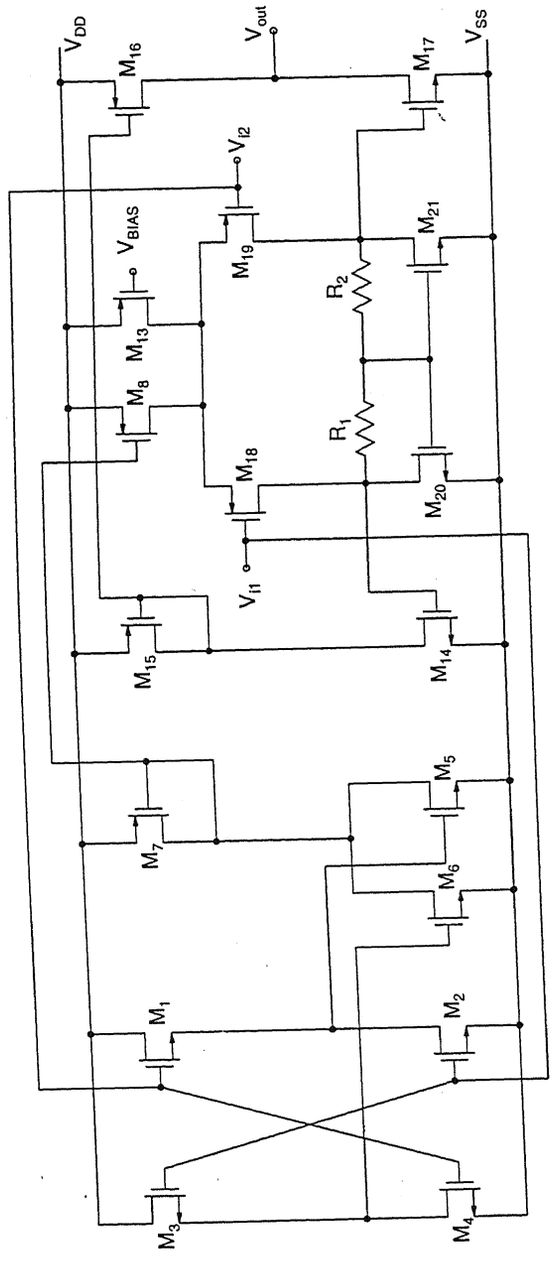

Figure 4.8. The schematic of the same OTA as shown in Fig.4.7, but now with adaptive biasing.

Table 4.2. W/L ratios of the MOSFETs used in the OTA shown in Fig.4.7.

Transistor Name	W/L Ratios (μm/μm)
M_{14}, M_{17}, M_{20}, M_{21}	120/1
M_{13}	100/1
M_{15}, M_{16}	240/1
M_{18}, M_{19}	50/1

V_{BIAS}. In the stand-by mode, the proposed adaptive biasing circuit provides very little current as compared to the current provided by the constant current source. Thus, g_m and r_d of the transistors used in the OTA remain the same as before, and hence, the small-signal response of the circuit remains unaffected. Figures 4.9 and 4.10 show the gain and phase responses of the OTA without adaptive biasing and with adaptive biasing respectively. Both these curves are identical as was expected, which substantiates the fact that the adaptive biasing block has no effect on the small-signal response of the circuit.

In order to obtain the dc transfer curve of these OTAs, the input V_{i1} is varied from −1 V to +1 V. The dc transfer curves of the OTA without and with adaptive biasing are shown in Figs.4.11 and 4.12 respectively. It is observed that the output range of the OTA of Fig.4.7 is from −915 mV to +913 mV, while that of the OTA of Fig.4.8 is from −902 mV to +907 mV. Thus, the output range is almost unaffected by the inclusion of the adaptive biasing block. The small reduction in the output range is due to the nonlinearity introduced by the adaptive biasing block. In order to obtain the transient response of these OTAs, an input square wave of 0.25 MHz frequency with an amplitude of ±1 V is applied at the input V_{i1} while keeping the other input grounded. A load capacitance C_L of 1 pF is used for obtaining the transient response and the slew rate characteristics. Figures 4.13 and 4.14 show the transient response of the OTAs without and with the adaptive

biasing block respectively, subjected to the same step input described earlier. It can be seen from these figures that the transient performance of the adaptively biased OTA is far superior than that of the OTA without adaptive biasing.

The settling time of the output of the OTA has decreased from 684 ns to only 1.61 ns for −1 V to +1 V transition, and from 1.28 μs to 15 ns for +1 V to −1 V transition. The positive slew rate has thus increased from 2.92 V/μs to 1242 V/μs, and the negative slew rate from 1.5625 V/μs to 133 V/μs. The power supply rejection ratio (PSRR) is defined as the product of the ratio of the change in the supply voltage to the change in the output voltage, and the open-loop gain of the op-amp. PSRR is a small-signal phenomenon, and thus, it also remains unaffected with the addition of the adaptive biasing circuit. The PSRR+ is 28.83 dB and PSRR− is 78.34 dB for both with and without adaptive biasing circuit. The noise spectral density at 100 KHz is same for both without and with adaptive biasing circuit & is equal to 2.25 $\mu V/\sqrt{Hz}$. The most interesting feature of this adaptive biasing circuit is that it requires negligible amount of additional quiescent power, which is approximately only 250 nW. Moreover, the additional transistor count is also very low, resulting in lesser area overhead requirements and lesser amount of noise introduction. Table 4.3 shows the comparison of the critical circuit parameters for the OTA without and with adaptive biasing. It is clear from this table that the adaptive biasing circuit has improved the dynamic performance of the OTA without adversely affecting other parameters too much. Table 4.4 shows the simulated total harmonic distortion for different amplitudes of a 100 KHz input sinusoidal wave. From Table 4.4, it can be inferred that the proposed circuit has no effect on the total harmonic distortion of the OTAs.

It is obvious from the results presented in this section that the proposed adaptive biasing circuit has substantially improved the dynamic performance of the OTA, without affecting the small-signal characteristics adversely. The stand-by power requirement of the adaptive biasing circuit is very low,

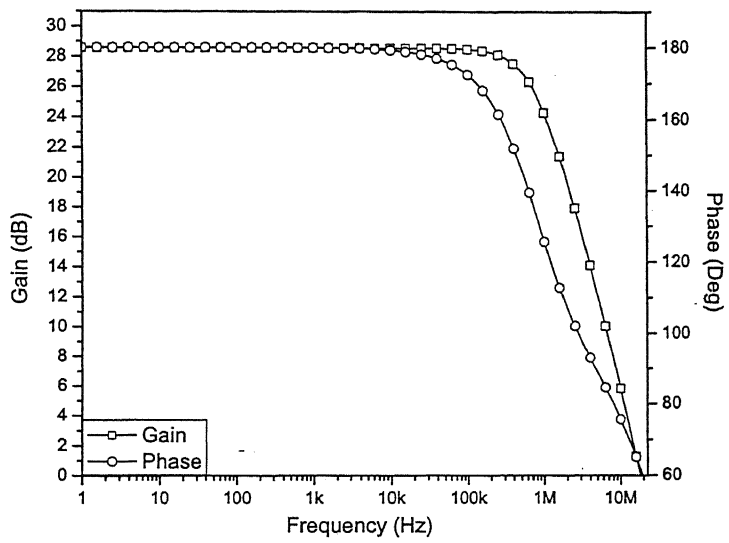

Figure 4.9. Gain and phase response of the OTA without adaptive biasing.

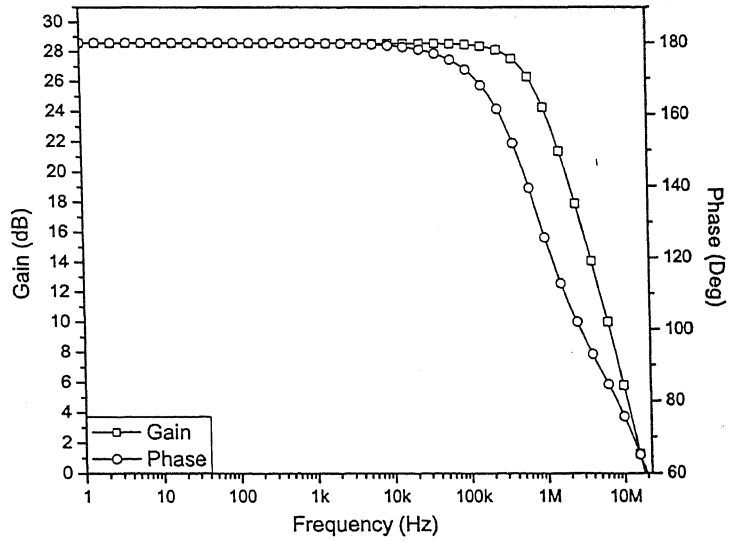

Figure 4.10. Gain and phase response of the OTA with adaptive biasing.

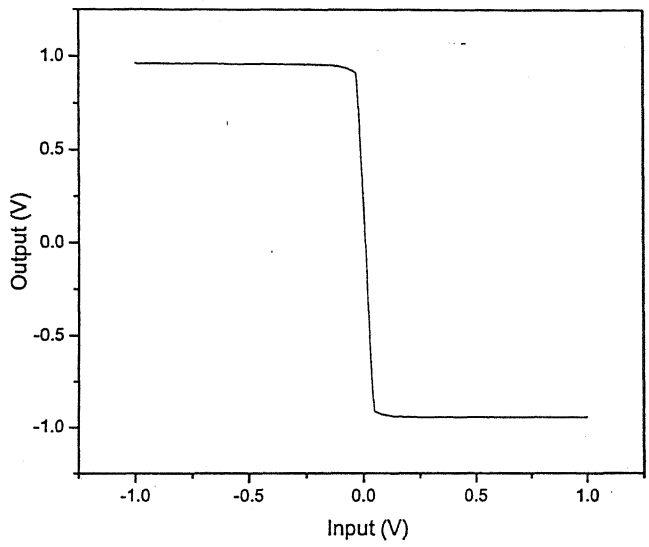

Figure 4.11. DC transfer curve of the OTA without adaptive biasing.

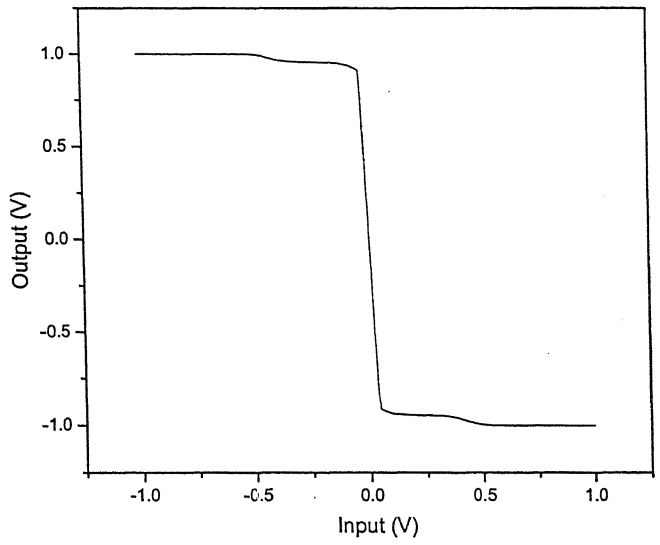

Figure 4.12. DC transfer curve of the OTA with adaptive biasing.

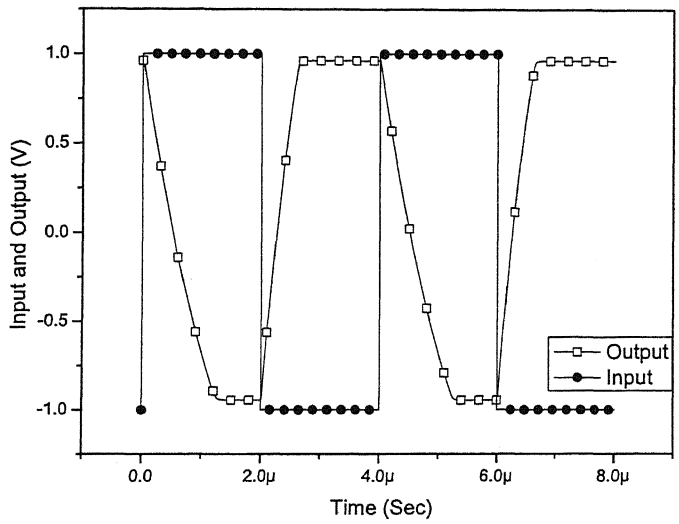

Figure 4.13. Transient response of the OTA without adaptive biasing.

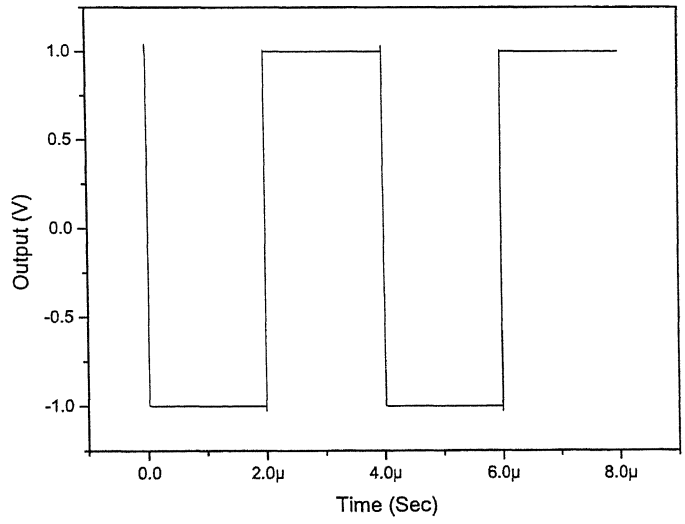

Figure 4.14. Transient response of the OTA with adaptive biasing, for the same input as shown in Fig.4.13.

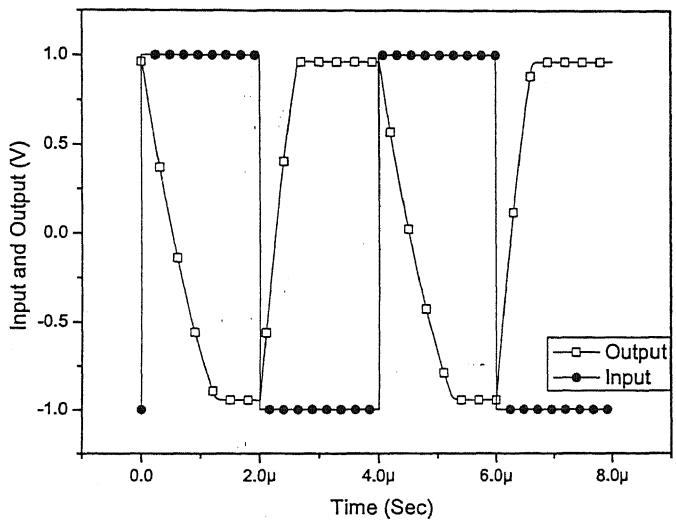

Figure 4.13. Transient response of the OTA without adaptive biasing.

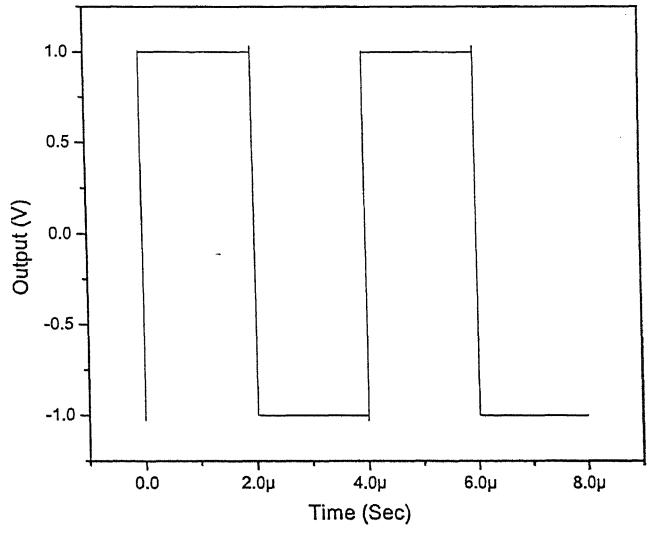

Figure 4.14. Transient response of the OTA with adaptive biasing, for the same input as shown in Fig.4.13.

Table 4.3. Performance comparison of an OTA with and without adaptive biasing.

Parameters	OTA Without Adaptive Biasing	OTA With Adaptive Biasing
DC Gain	28.2 dB	28.2 dB
GBP	18.23 MHz	18.23 MHz
Positive Slew Rate	2.92 V/μs	1242 V/μs
Negative Slew Rate	1.5625 V/μs	133 V/μs
$PSRR+$	28.83 dB	28.83 dB
$PSRR-$	78.34 dB	78.34 dB
Noise Spectral Density at 100 KHz	2.25 μV/$\sqrt{Hz}$	2.25 μV/$\sqrt{Hz}$
Static Power Dissipation	27.30 μW	27.55 μW
Output Range	-915 mV to +913 mV	-902 mV to +907 mV

thereby making it suitable for low-power applications. The proposed adaptive biasing circuit uses a very low number of transistors, thus not penalizing Si area requirements too much.

Table 4.4. Total Harmonic Distorton (THD) of an OTA with and without adaptive biasing.

Amplitude of Input Sine-Wave	THD of OTA Without Adaptive Biasing (%)	THD of OTA With Adaptive Biasing (%)
5 mV	0.52	0.52
15 mV	0.57	0.56
25 mV	2.53	2.54
35 mV	9.17	9.18
45 mV	14.94	14.94

Chapter 5

Conclusion and Scope for Future Work

5.1 Conclusion

Widespread use of battery-operated systems has given rise to an increased demand for low-voltage, low-power circuits, in the search for less weight and size and extended operative lifetime of the batteries. In this context, it is critical to preserve the dynamic performance of analog circuits with both minimum supply voltage and minimum stand-by power consumption. Adaptive biasing circuits are very useful in such situations. They provide a variable bias current only in the presence of a differential input signal. In the absence of any differential input signal, they provide a constant quiescent current, which can be accurately controlled. In this way, the static power consumption is reduced without compromising the transient behavior. In the literature, several adaptive biasing circuits have been proposed, however, almost all of them require additional quiescent current sources, thereby making the stand-by power consumption of the overall circuit considerable. Adaptive biasing circuits, which do not require any additional quiescent current sources, are also available, however, their sensitivity to the input signals is quite poor. In order to improve the sensitivity of these circuits,

again additional quiescent current sources are required.

In this work here, a new adaptive biasing circuit for DAs has been proposed, which does not require any quiescent current source. The designed circuit has been used in an Operational Transconductance Amplifier (OTA). In order to reduce the power consumption of the OTA, the MOSFETs contained therein are operated in their subthreshold region of operation, with a total biasing curent of only 5 μA. The power supplies used are $\pm$1 V. It has been shown that with the addition of the proposed adaptive biasing block, the dynamic performance of the OTA can be improved without adversely affecting the other circuit parameters too much. The proposed adaptive biasing circuit takes only 250 nW of additional power. The positive slew rate has improved from 2.92 V/μs to 1242 V/μs, and the improvement in the negative slew rate is from 1.5625 V/μs to 133 V/μs for a capacitive load of 1 pF. The settling time for a −1 V to +1 V transition of the output has been decreased from 1.28 μs to 15 ns, and for a +1 V to −1 V transition it has come down to 1.61 ns from 684 ns. The gain-bandwidth-product of the circuit remains unaffected and is equal to 18.23 MHz for both the cases. The output voltage range has been affected negligibly. It was −915 mV to +913 mV for the OTA without adaptive biasing and −902 mV to +907 mV with adaptive biasing. The noise spectral density at 100 KHz is same for both without and with adaptive biasing circuit and is equal to 2.25 $\mu V/\sqrt{Hz}$. The PSRR also remains unaffected with the addition of the proposed biasing circuit, i.e., PSRR+ is 28.83 dB and PSRR− is 78.34 dB for both the cases. The proposed biasing circuit has no effect on the total harmonic distortion (THD) of the circuit for small amplitudes of input sine-wave.

5.2 Scope for Future Work

In this work, the proposed adaptive biasing circuit has been used to improve the dynamic performance of the unbuffered op-amps (OTAs), however, the

same circuit can be utilized to improve the dynamic performance of the buffered op-amps as well. A voltage follower (buffer) is necessary in many applications. However, these buffers have very high power consumption. The proposed adaptive biasing topology can be used to design high slew-rate low-power voltage buffers, where the dynamic characteristics of the buffers can be improved without heavy power dissipation except for a very short time interval during which the signal is present. The biasing circuit can also be useful for high speed data converters. The proposed adaptive biasing circuit has been operated with ± 1 V power supply voltages. However, it can also be operated at lower supply voltages. Single power supply can also be used instead of the dual supply voltages used here. The proposed adaptive biasing circuit can be used to provide a programmable bias current. In order to make a programmable adaptive biasing current source, additional transistors can be connected in parallel with the transistors M_{10} of Fig.4.1, however, drains of these transistors will be connected to the drain of M_{10} through switches. These swithches can be operated using digital signals thereby making the circuit a programmable adaptive biasing circuit.

APPENDIX

NMOS

0.5 μm Technology File

.MODEL CMOSN NMOS LEVEL = 49

+VERSION = 3.1 TNOM = 27 TOX = 9.6E-9

+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.627652

+K1 = 0.793853 K2 = -0.0306761 K3 = 78.5045537

+K3B = 0.1300339 W0 = 1E-5 NLX = 3.89825E-8

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 6.7330734 DVT1 = 0.8341494 DVT2 = -0.1360511

+U0 = 423.6054862 UA = 1E-12 UB = 1.365092E-18

+UC = 1.078475E-11 VSAT = 1.236292E5 A0 = 0.9417794

+AGS = 0.1494531 B0 = 1.565313E-6 B1 = 5E-6

+KETA = 2.243159E-3 A1 = 0 A2 = 1

+RDSW = 1.153603E3 PRWG = 0.0653342 PRWB = -0.0681133

+WR = 1 WINT = 2.329652E-7 LINT = 1.00611E-7

+XL = -1E-7 XW = 0 DWG = -4.464259E-9

+DWB = 1.245396E-8 VOFF = -0.0580692 NFACTOR = 1.4823566

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.043042 ETAB = -5.942602E-3

+DSUB = 0.4388988 PCLM = 0.6404859 PDIBLC1 = 1.514861E-7

+PDIBLC2 = 3.246207E-3 PDIBLCB = -0.197801 DROUT = 1.551814E-3

+PSCBE1 = 5.680232E9 PSCBE2 = 1.369852E-9 PVAG = 0.0306927

+DELTA = 0.01 RSH = 2.8 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 2.81E-10 CGSO = 2.81E-10 CGBO = 1E-9

+CJ = 5.04643E-4 PB = 0.99 MJ = 0.8099425

+CJSW = 4.814417E-10 PBSW = 0.99 MJSW = 0.1

+CJSWG = 2.2346E-10 PBSWG = 0.99 MJSWG = 0.1

+CF = 0 PVTH0 = 9.036446E-3 PRDSW = -22.8038789

+PK2 = 0.0105156 WKETA = -3.709225E-3 LKETA = -8.524366E-3

+PAGS = 0.0968

PMOS

0.5 μm Technology File

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+VERSION = 3.1 TNOM = 27 TOX = 9.6E-9
+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.8351513
+K1 = 0.3832927 K2 = 0.0182059 K3 = 93.9598487
+K3B = -5 W0 = 1E-5 NLX = 2.041534E-7
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 3.7095566 DVT1 = 0.5091225 DVT2 = -0.0368146
+U0 = 181.6646706 UA = 1.338606E-9 UB = 1.002605E-18
+UC = -5.64742E-11 VSAT = 2.234764E5 A0 = 0.9423567
+AGS = 0.2743733 B0 = 4.198245E-6 B1 = 5E-6
+KETA = 3.411785E-3 A1 = 0 A2 = 1
+RDSW = 3.5E3 PRWG = -0.0704989 PRWB = 5.293994E-3
+WR = 1 WINT = 2.285806E-7 LINT = 6.239413E-8
+XL = -1E-7 XW = 0 DWG = -1.628171E-8
+DWB = 9.20495E-9 VOFF = -0.0914053 NFACTOR = 0.9483204
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.0364279 ETAB = 3.484825E-3
+DSUB = 0.2648828 PCLM = 4.0562705 PDIBLC1 = 1.366583E-6
+PDIBLC2 = 6.468762E-3 PDIBLCB = -0.0188204 DROUT = 0
+PSCBE1 = 5.65221E9 PSCBE2 = 5.685284E-10 PVAG = 13.2742869
+DELTA = 0.01 RSH = 2.3 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WL = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.52E-10 CGSO = 2.52E-10 CGBO = 1E-9
+CJ = 9.379142E-4 PB = 0.9348647 MJ = 0.4765513
+CJSW = 1.279151E-10 PBSW = 0.99 MJSW = 0.1303972
+CJSWG = 4.256E-11 PBSWG = 0.99 MJSWG = 0.1303972
+CF = 0 PVTH0 = -1.076201E-3 PRDSW = 282.4948778
+PK2 = 3.181465E-3 WKETA = 7.931059E-3 LKETA = -9.663719E-3
+PAGS = 0.09532

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